

Fig. 1



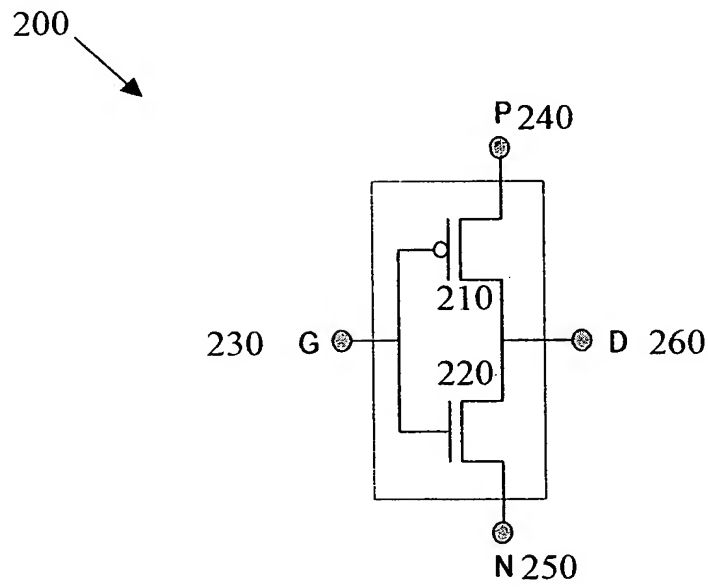


Fig. 2

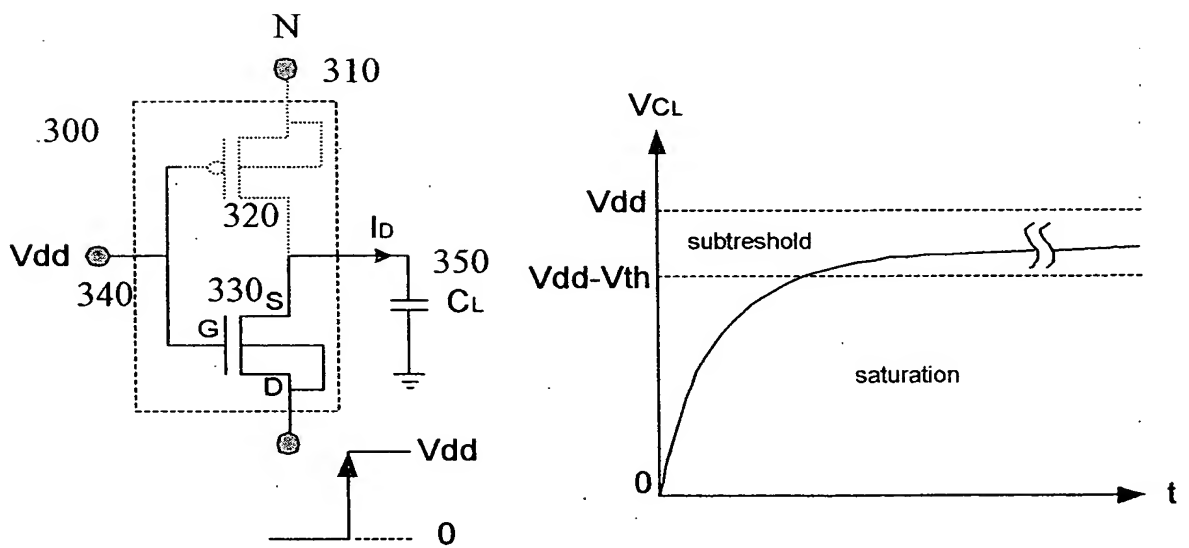


Fig. 3

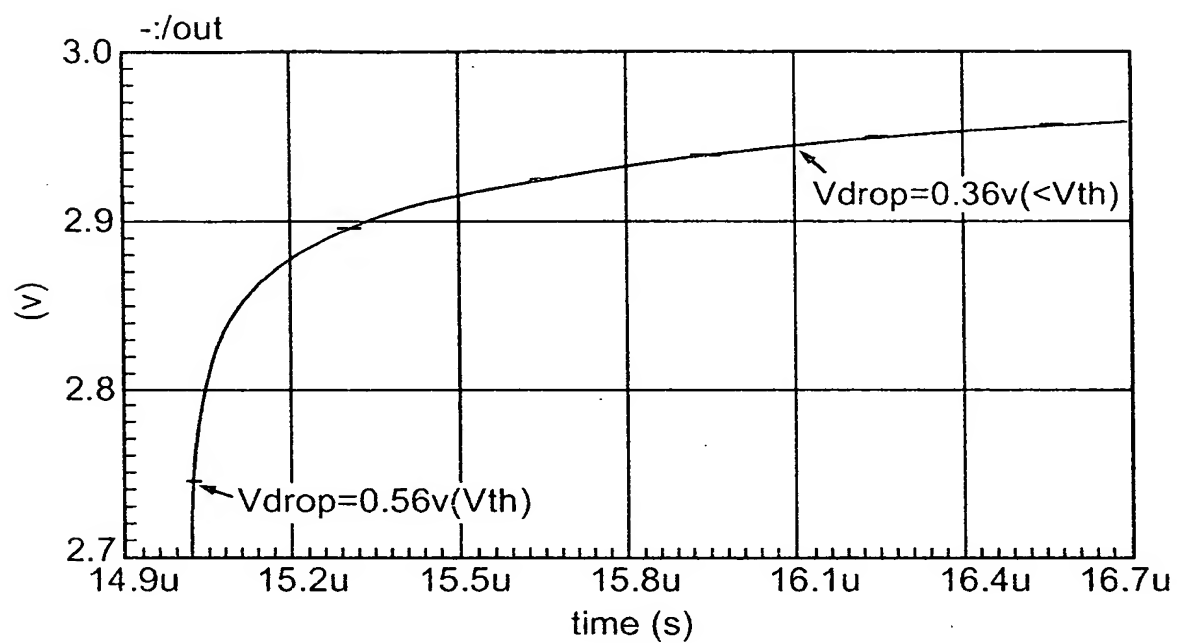


Fig. 4

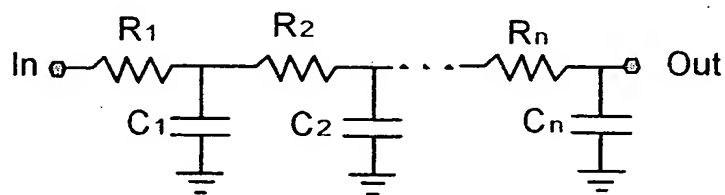


Fig. 5

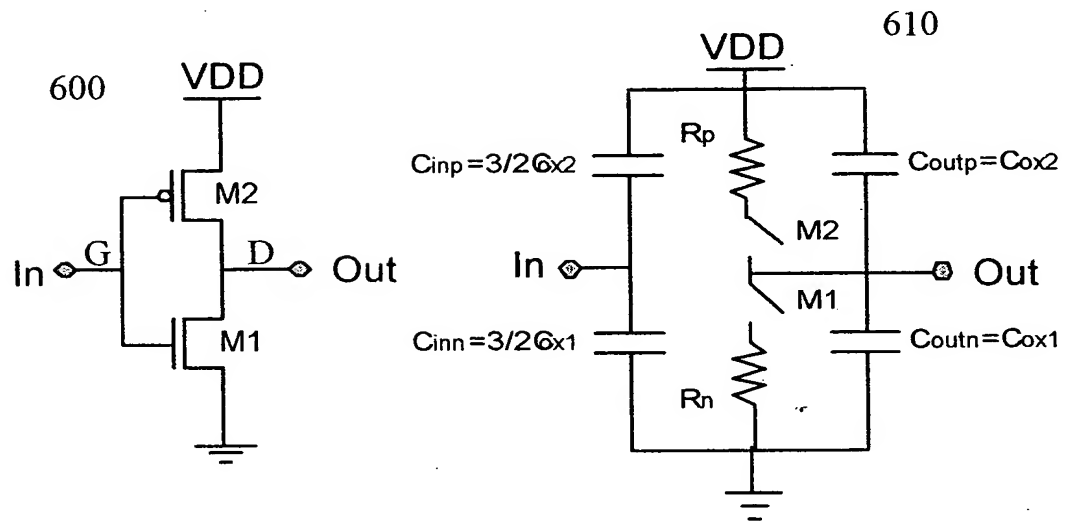
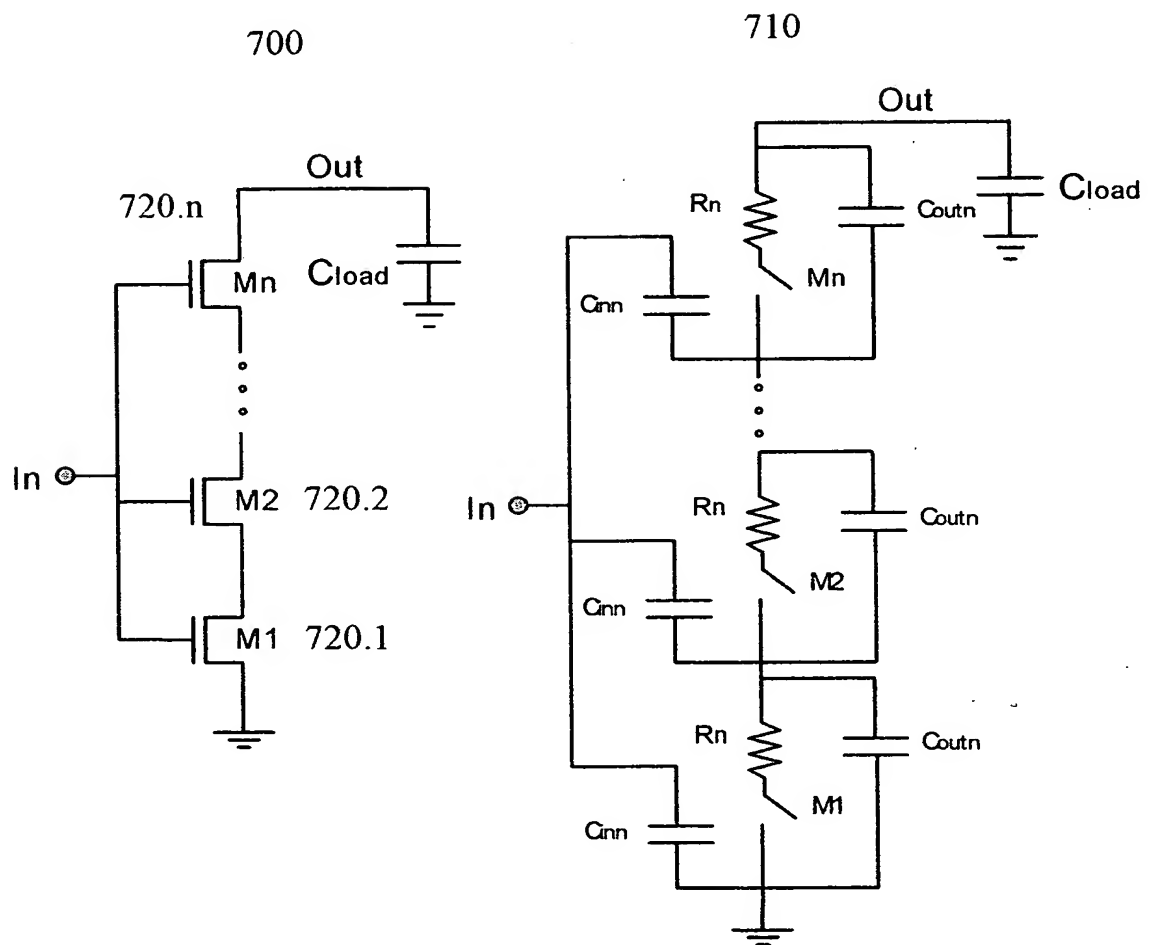


Fig. 6

**Fig. 7 - Prior art**

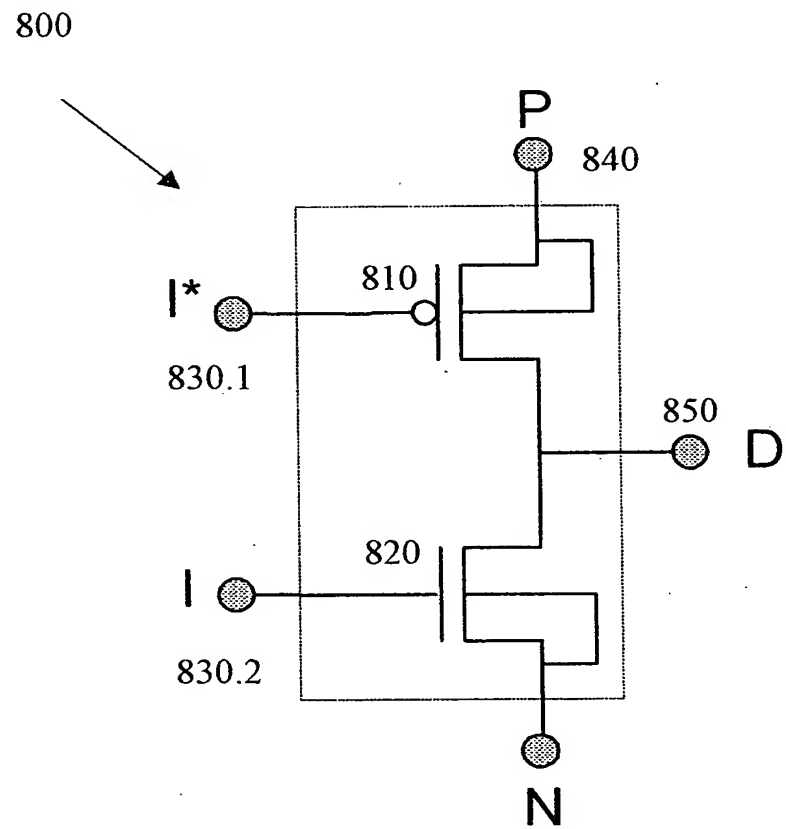
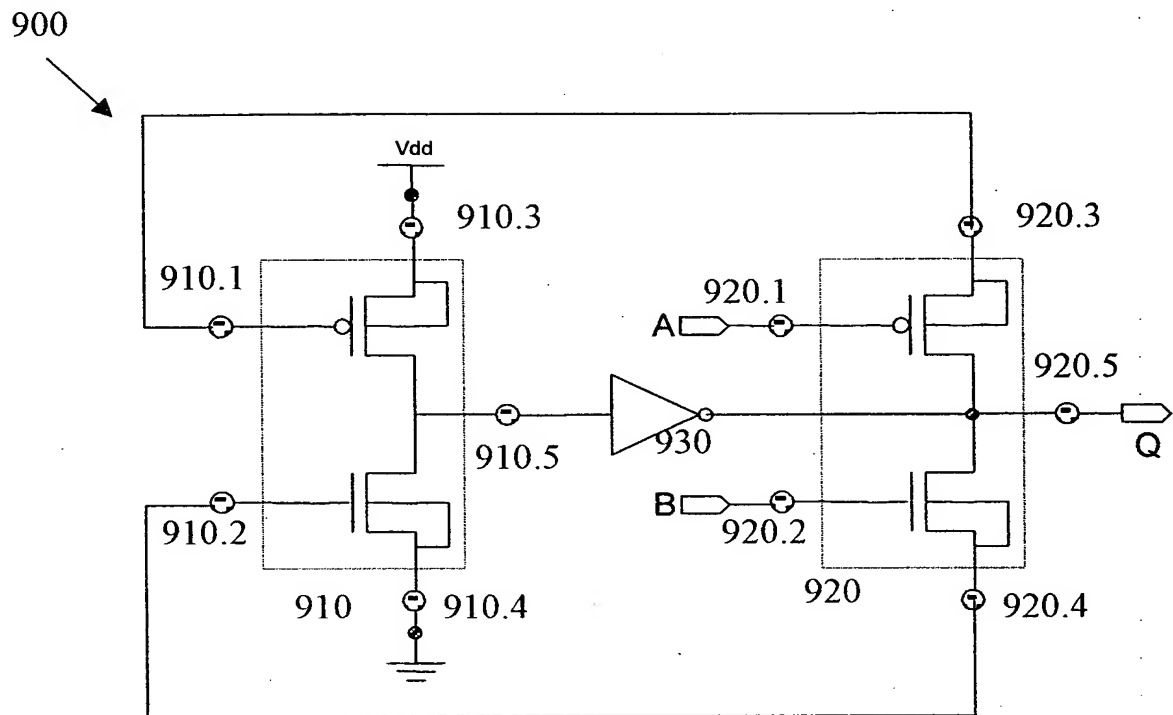


Fig. 8



**Fig. 9**

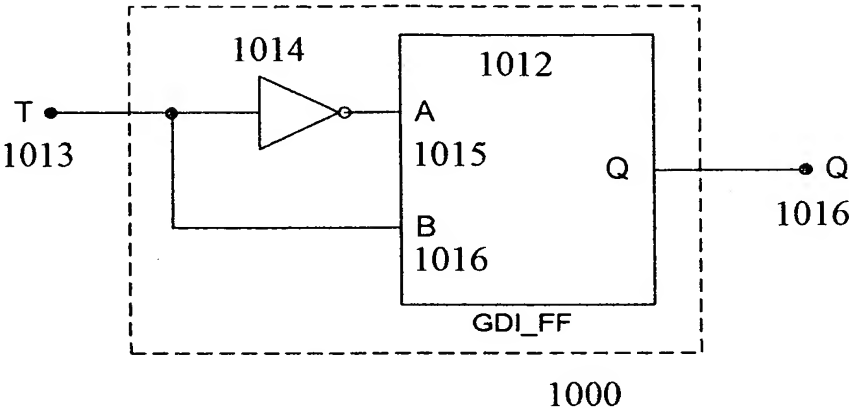


Fig. 10a

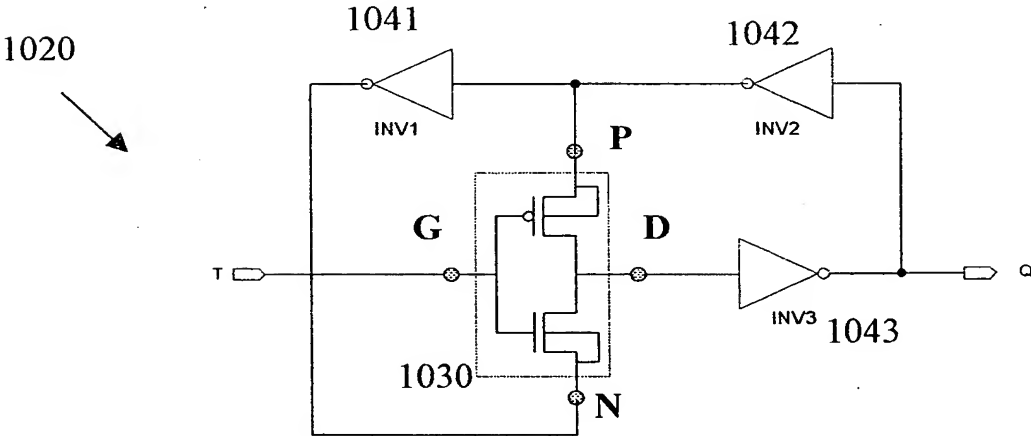


Fig. 10b



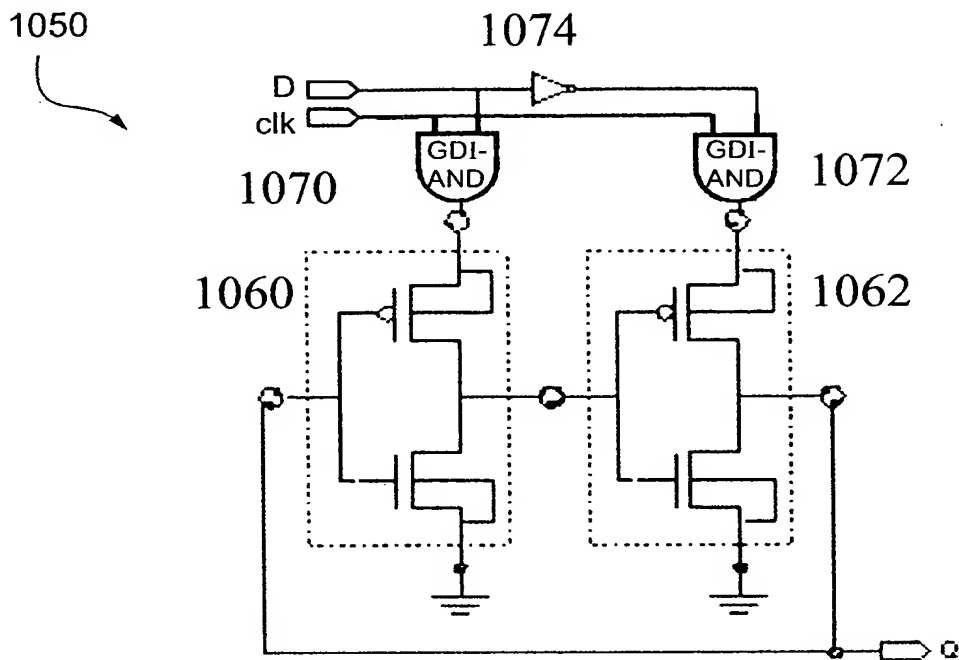


Fig. 10c

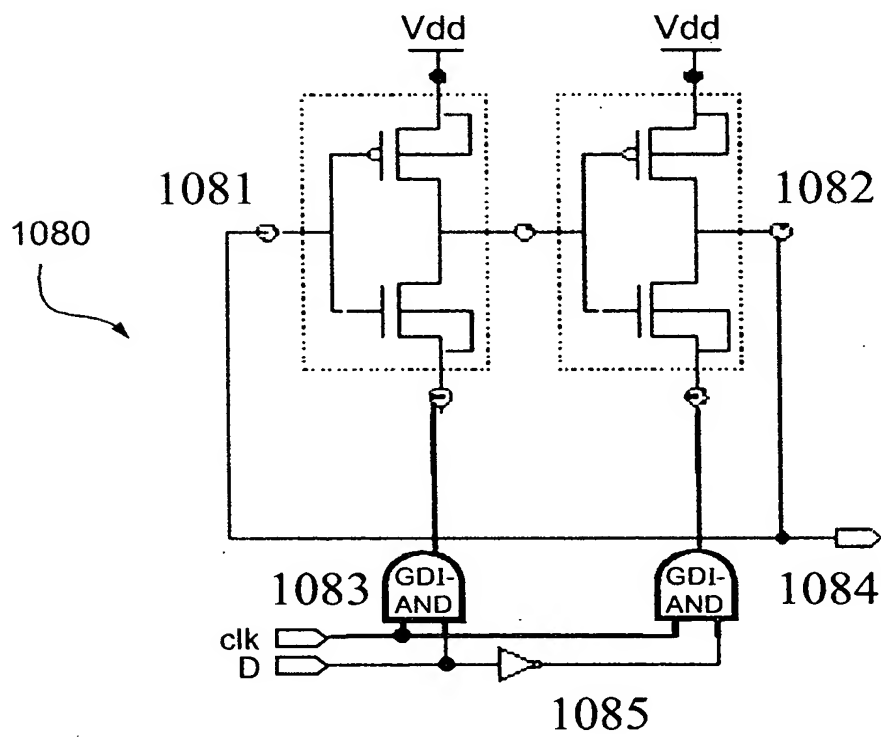


Fig. 10d

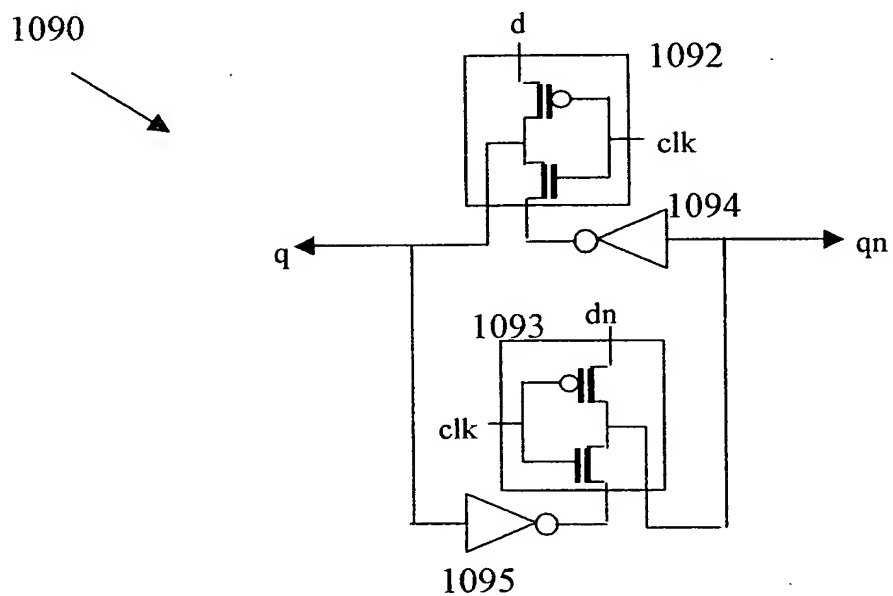


Fig. 10e

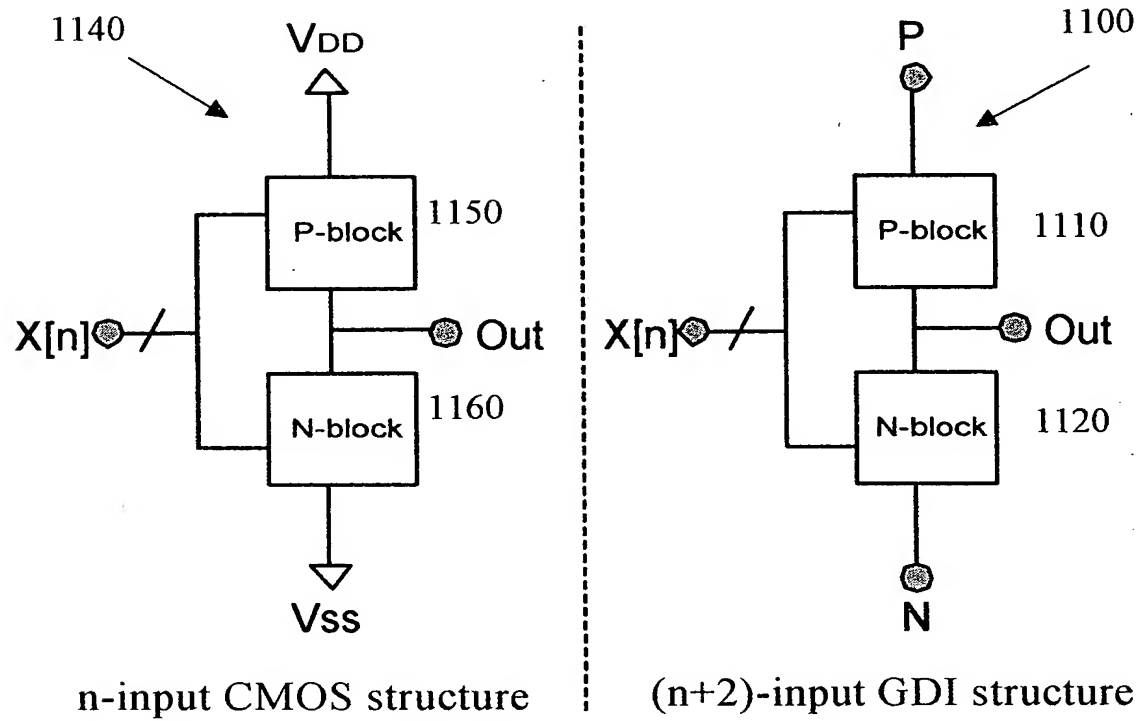
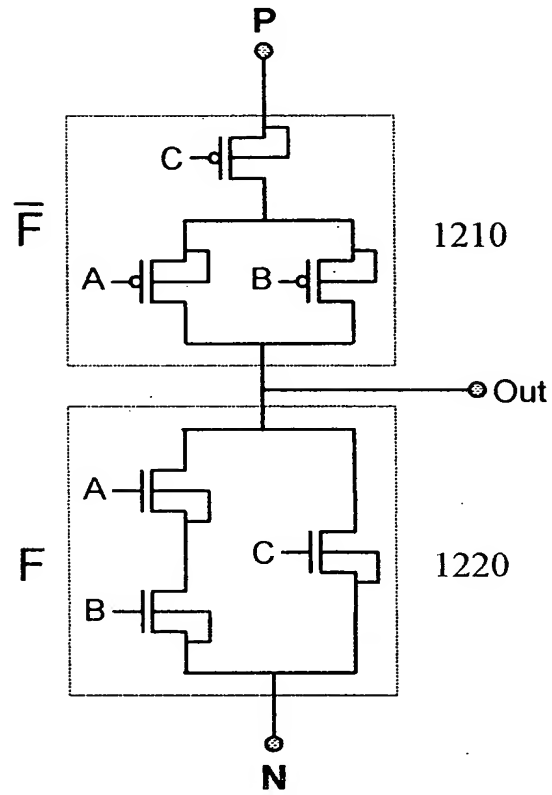


Fig. 11

1200



$$\text{Out} = \overline{F}P + FN = \overline{(AB+C)}P + (AB+C)N$$

Fig. 12

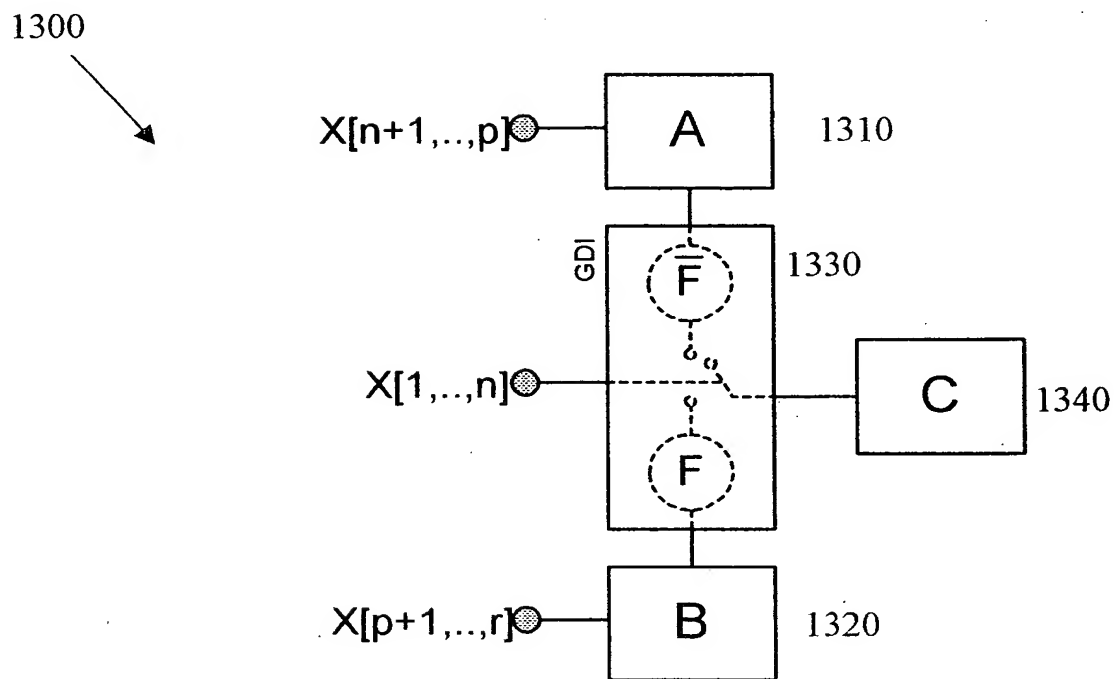
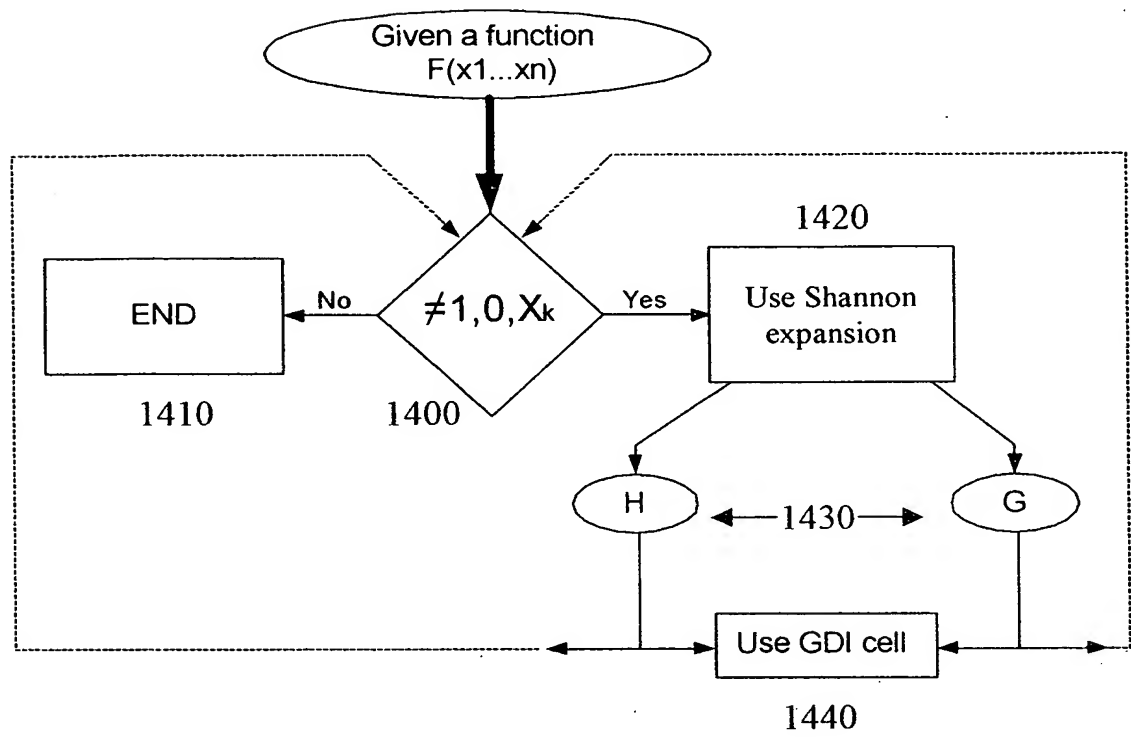


Fig. 13

**Fig. 14**

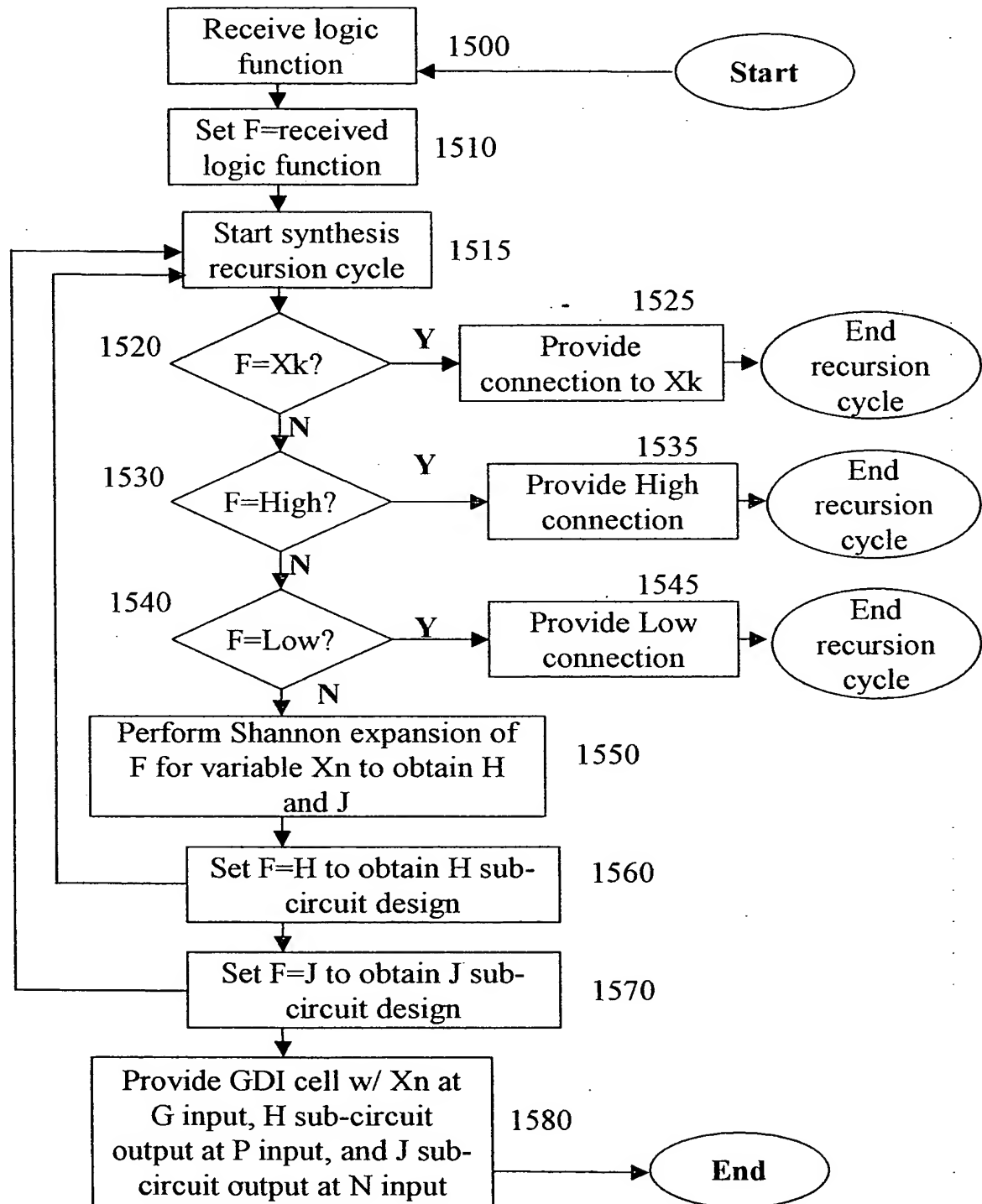
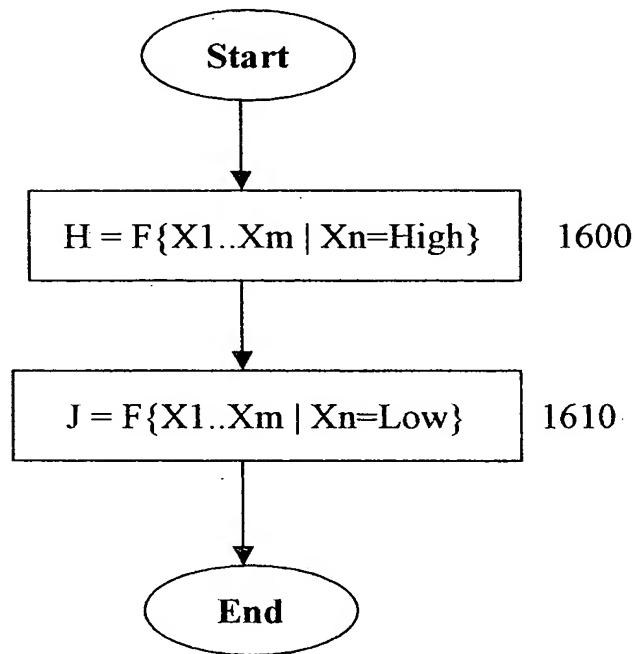
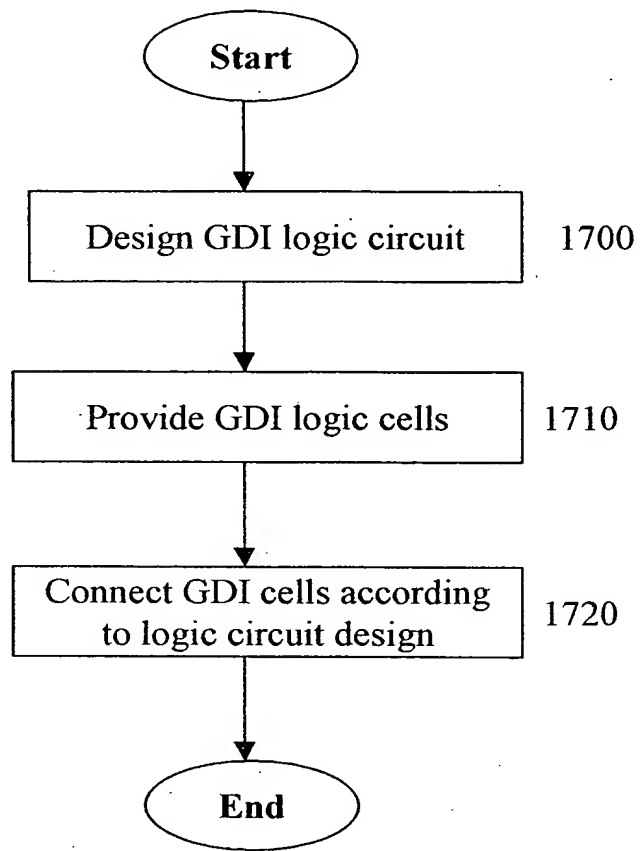


Fig. 15

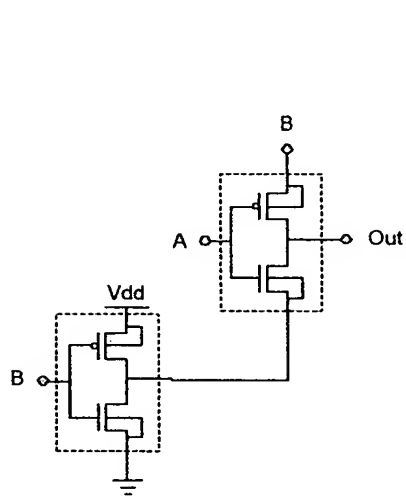


**Fig. 16**

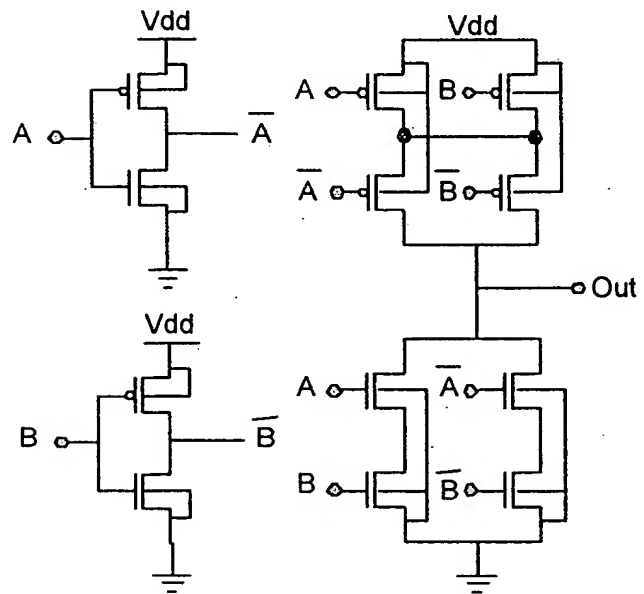




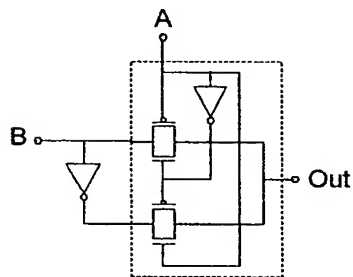
**Fig. 17**

**GDI**

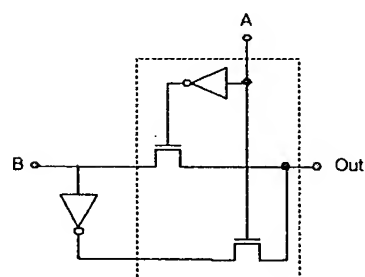
4 transistors

**CMOS – Prior art**

12 transistors

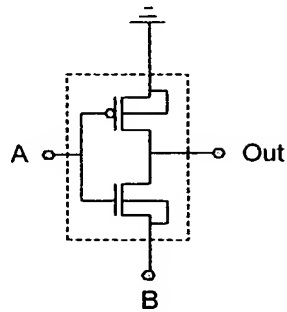
**TG – Prior art**

8 transistors

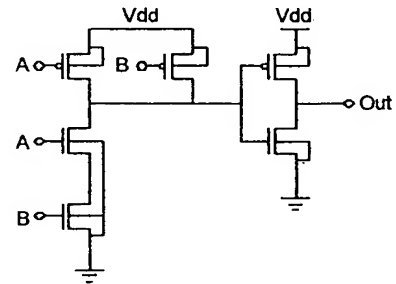
**N-PG – Prior art**

6 transistors

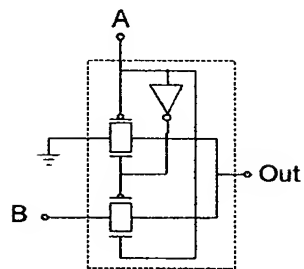
**XOR gate****Fig. 18a**



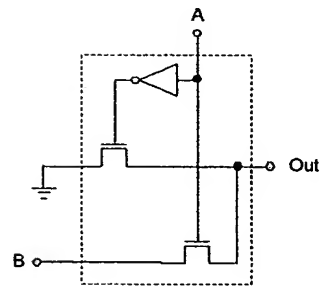
**GDI**  
2 transistors



**CMOS - Prior art**  
6 transistors



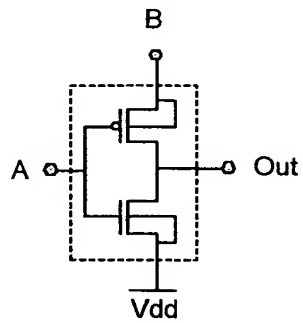
**TG - Prior art**  
6 transistors



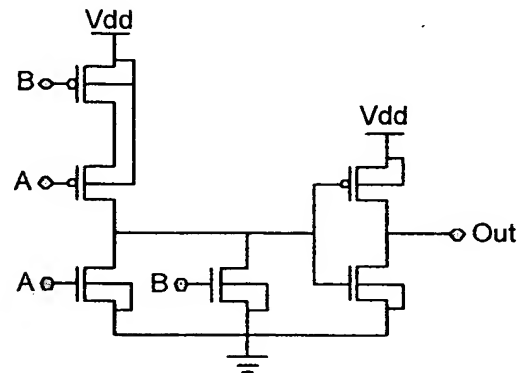
**N-PG - Prior art**  
4 transistors

**AND gate**

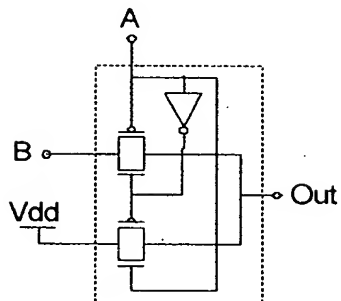
**Fig. 18b**



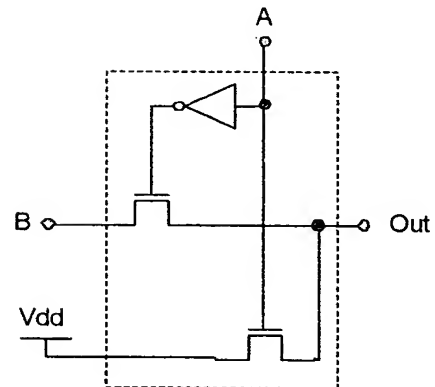
**GDI**  
2 transistors



**CMOS - Prior art**  
6 transistors



**TG - Prior art**  
6 transistors



**N-PG - Prior art**  
4 transistors

**OR gate**

**Fig. 18c**

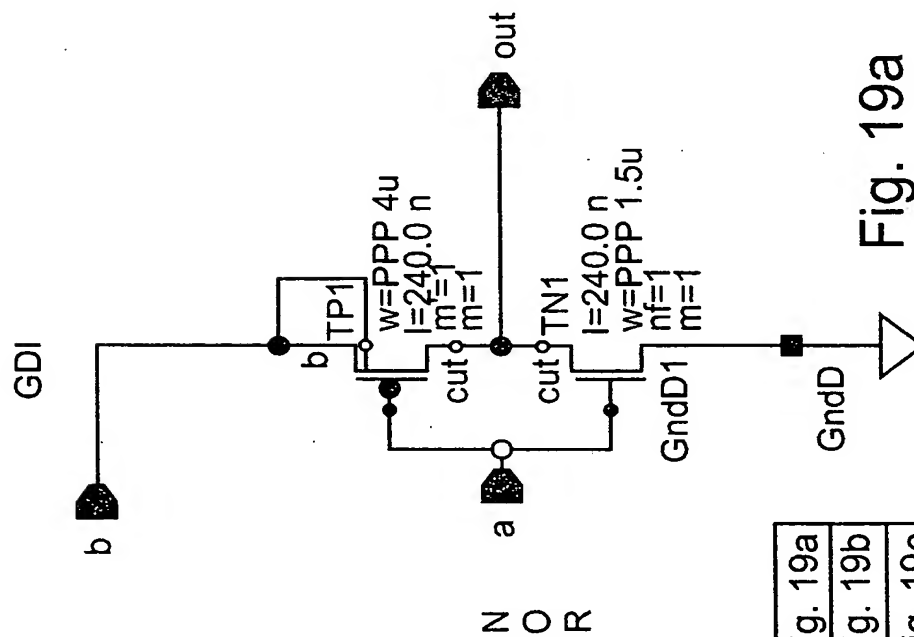


Fig. 19a

Power (DUT and driver) vs. load size

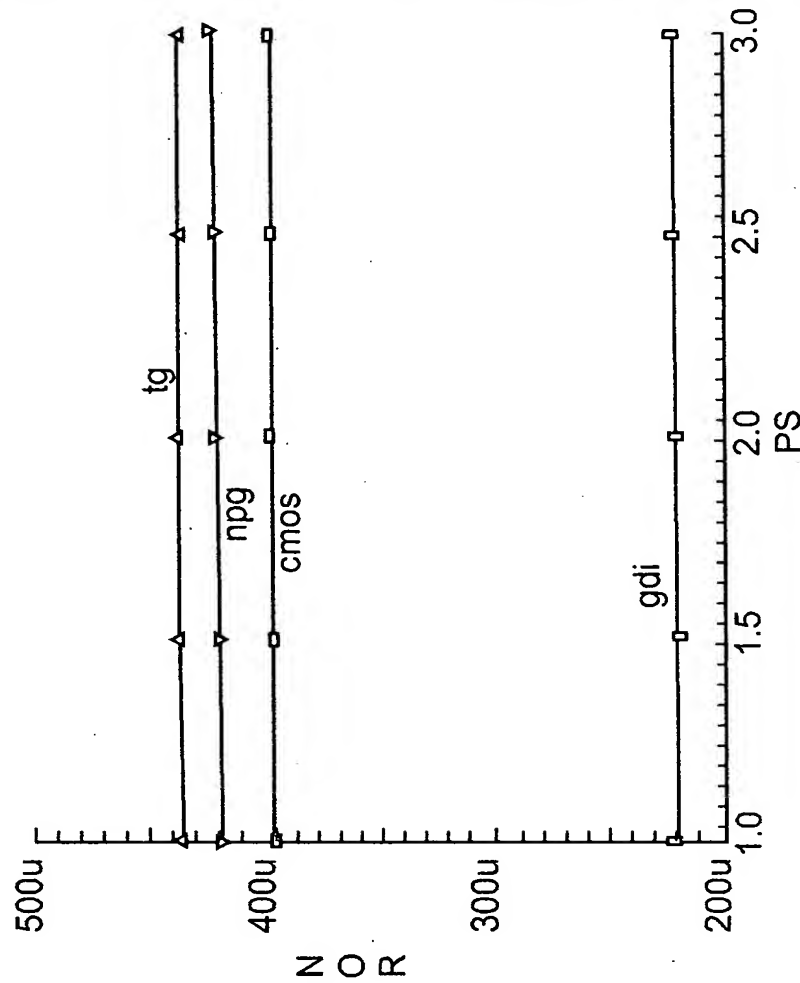


Fig. 19b

Fig. 19a
Fig. 19b
Fig. 19c
Fig. 19d
Fig. 19e
Fig. 19f

Fig. 19

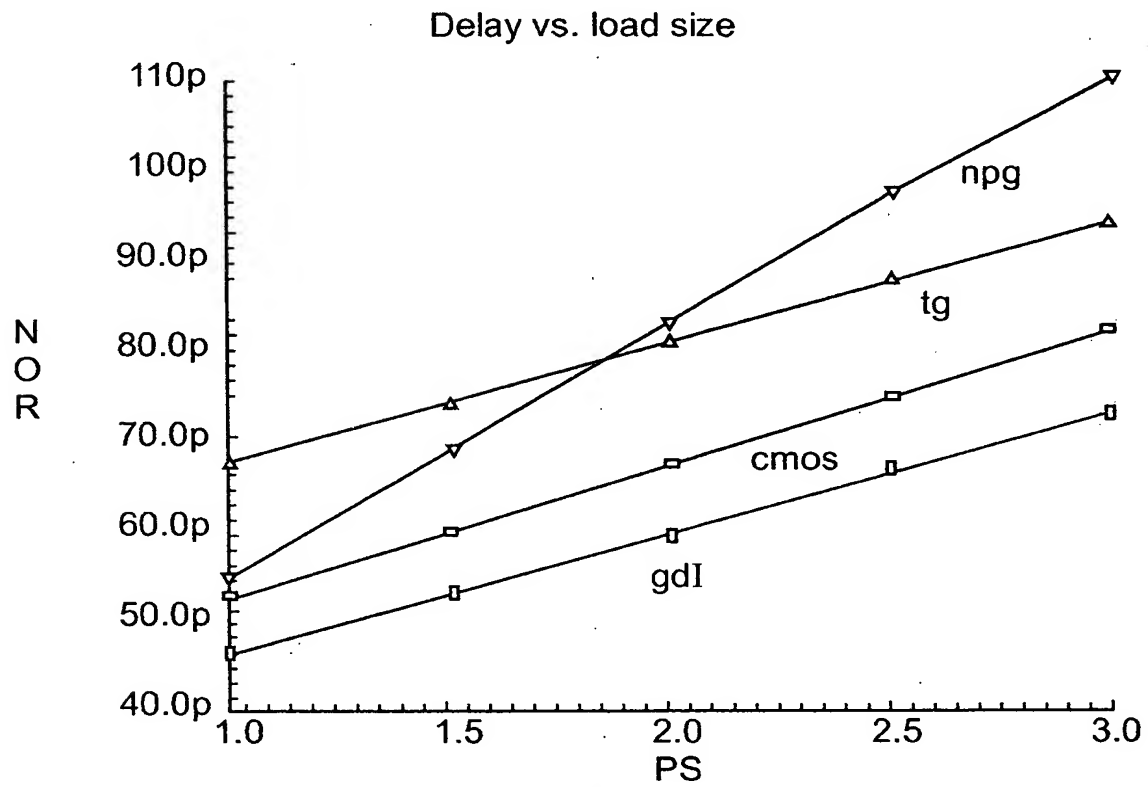
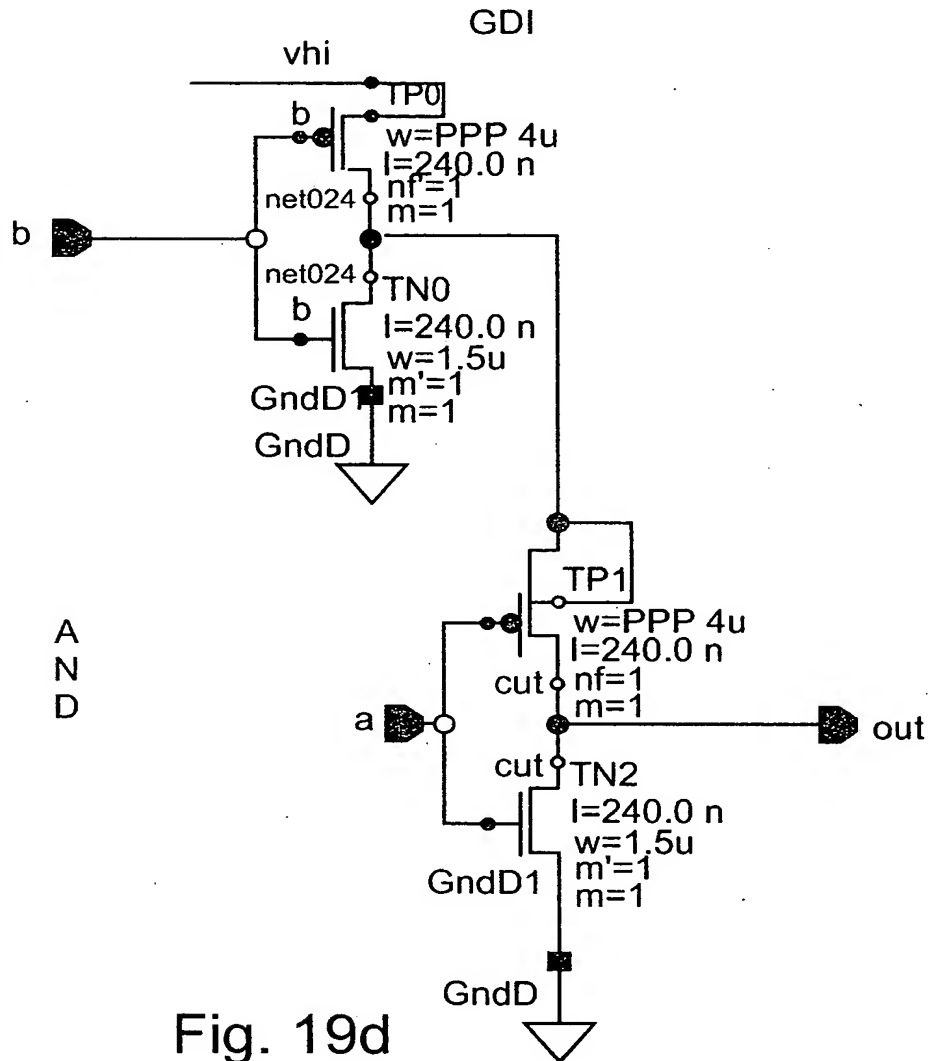


Fig. 19c



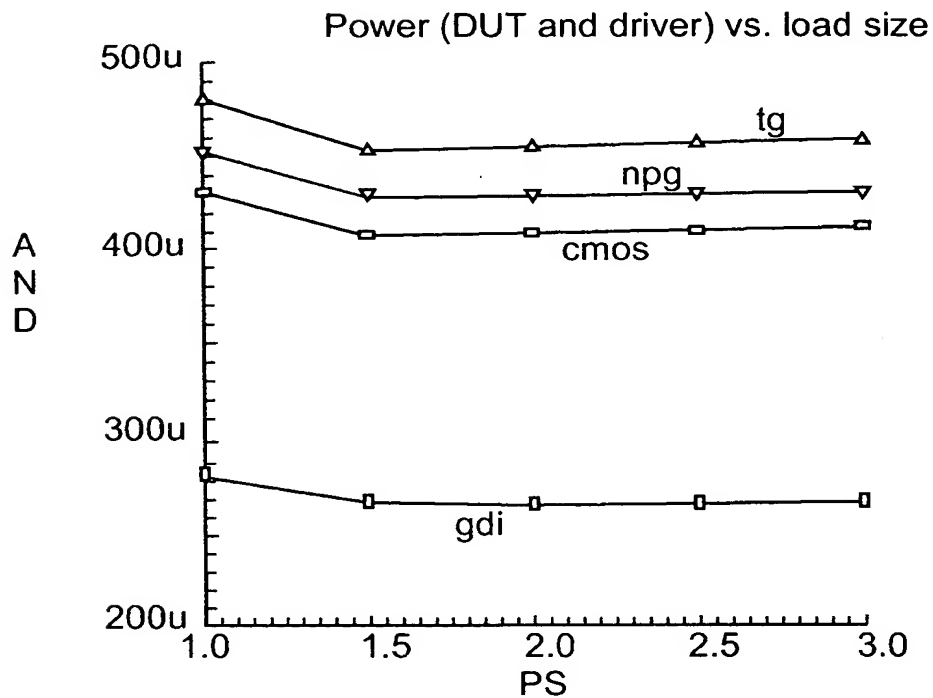


Fig. 19e

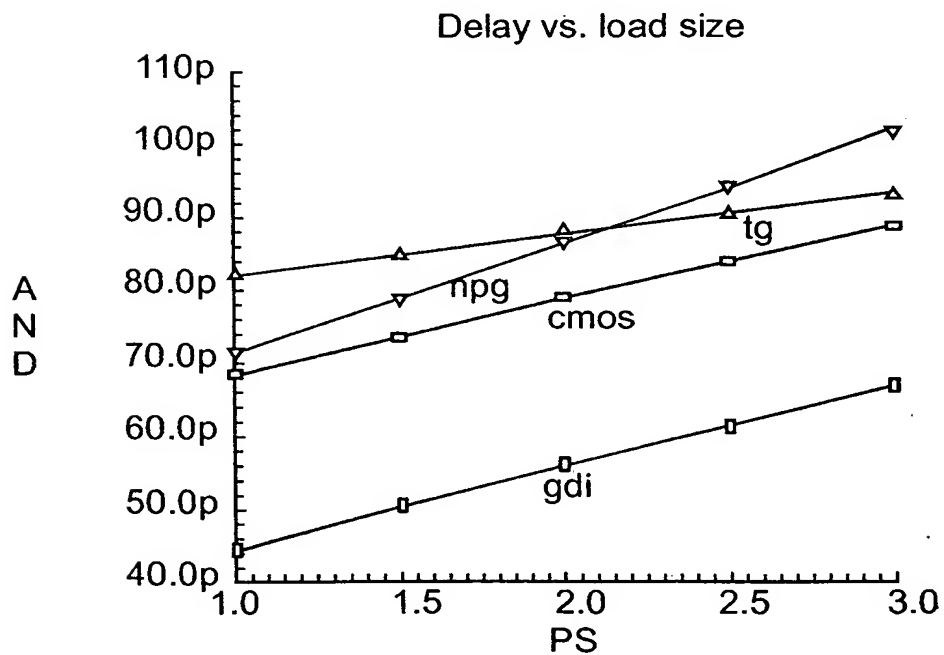


Fig. 19f



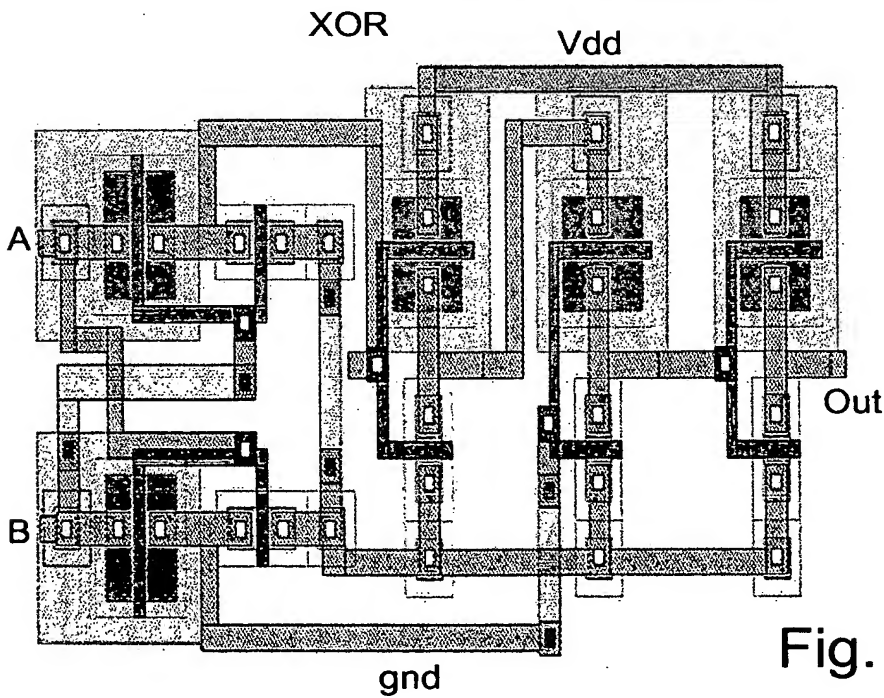
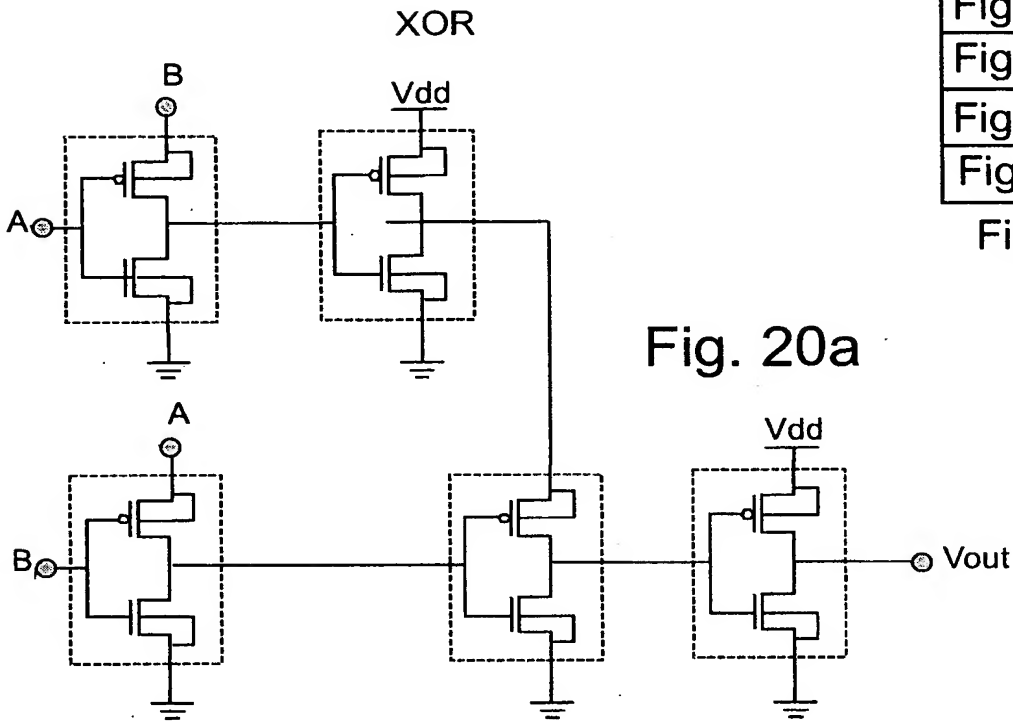


Fig. 20a
Fig. 20b
Fig. 20c
Fig. 20d
Fig. 20e
Fig. 20f

Fig. 20

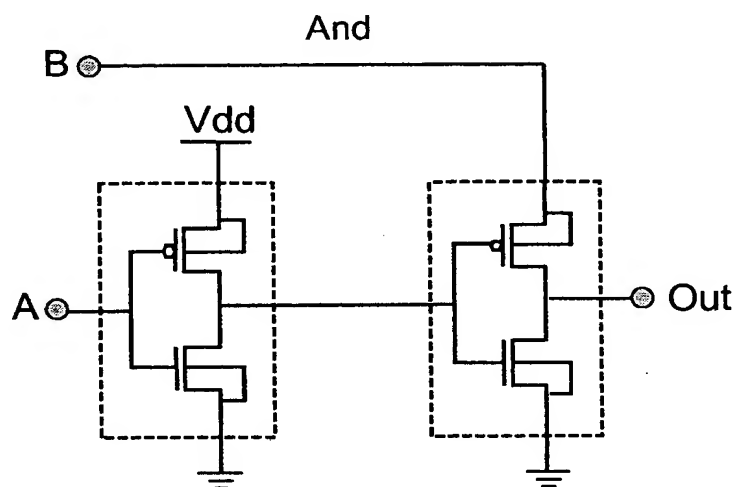


Fig. 20c

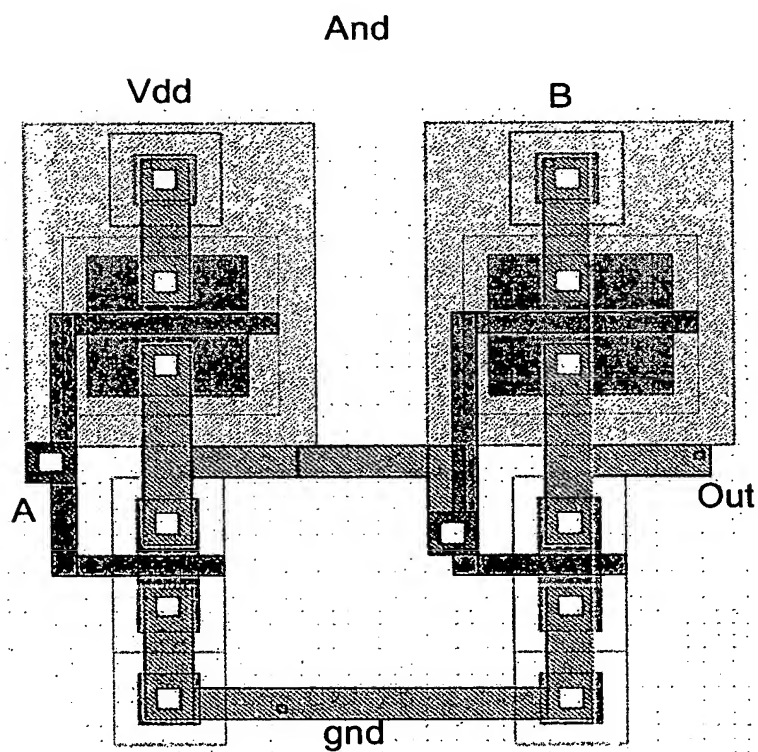


Fig. 20d

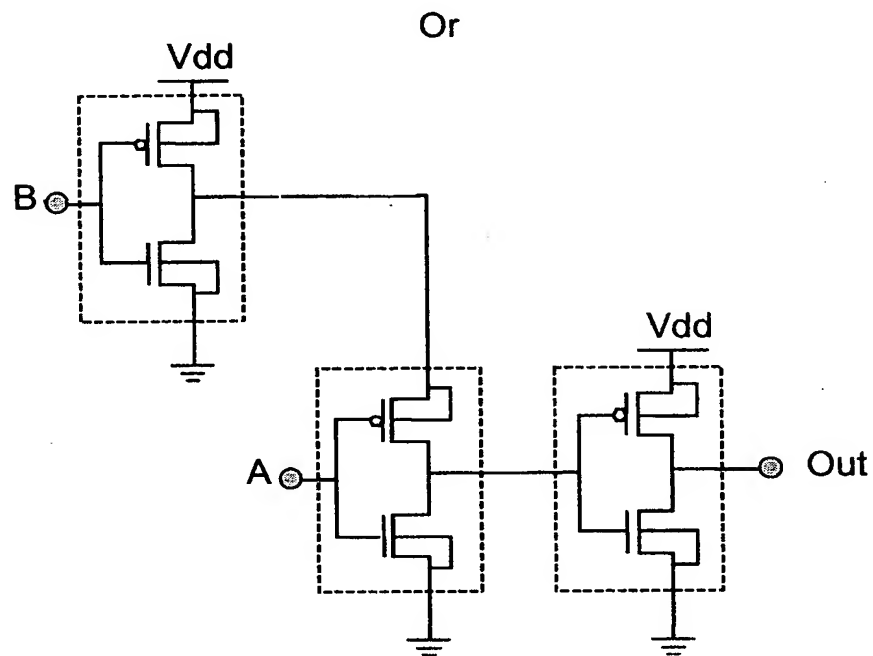


Fig. 20e

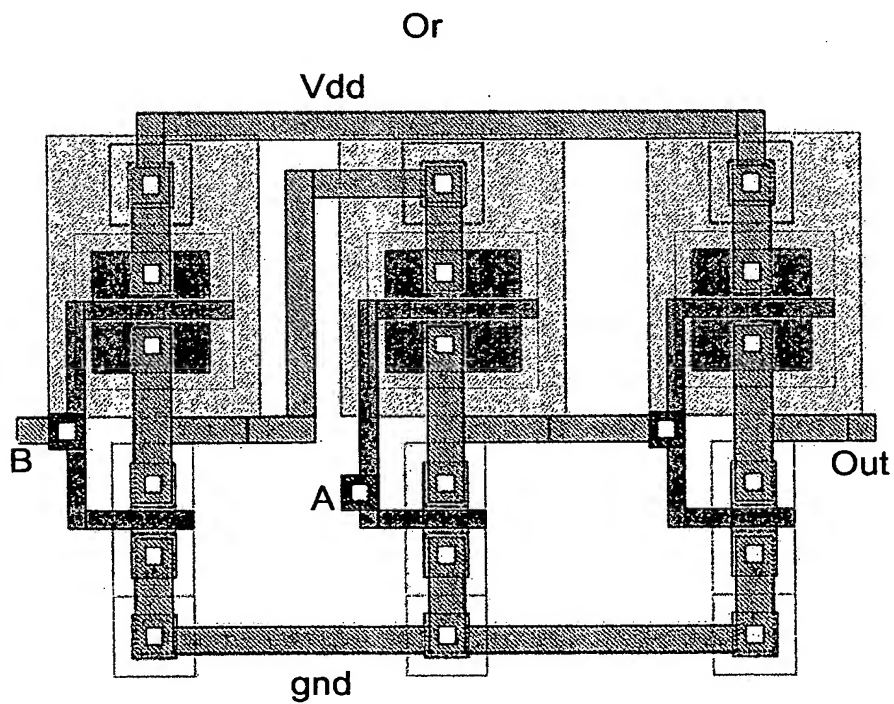
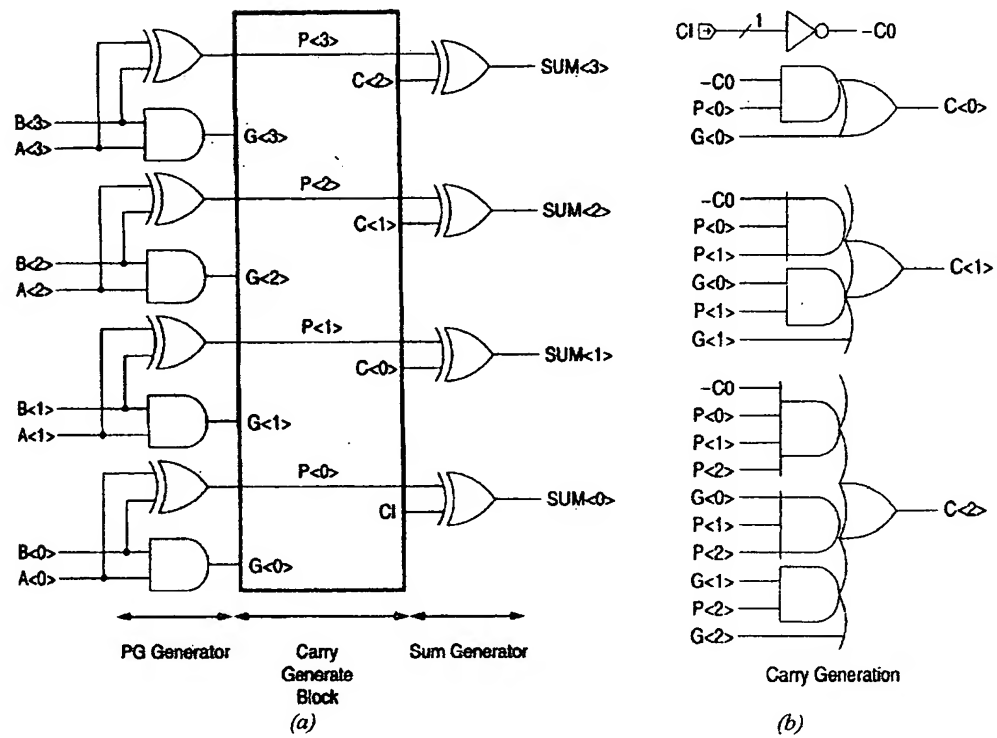


Fig. 20f



a) Basic scheme

b) Carry Generator  
(3-bit only)

Fig. 21 – Prior art

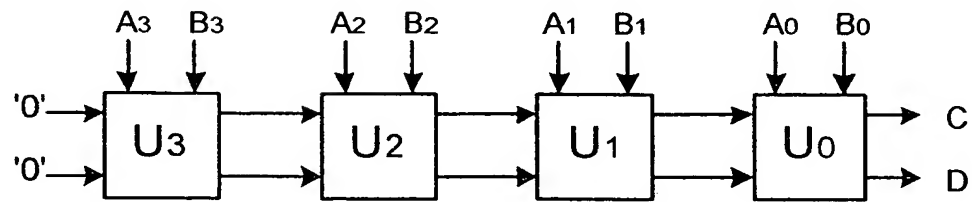


Fig. 22 – Prior art

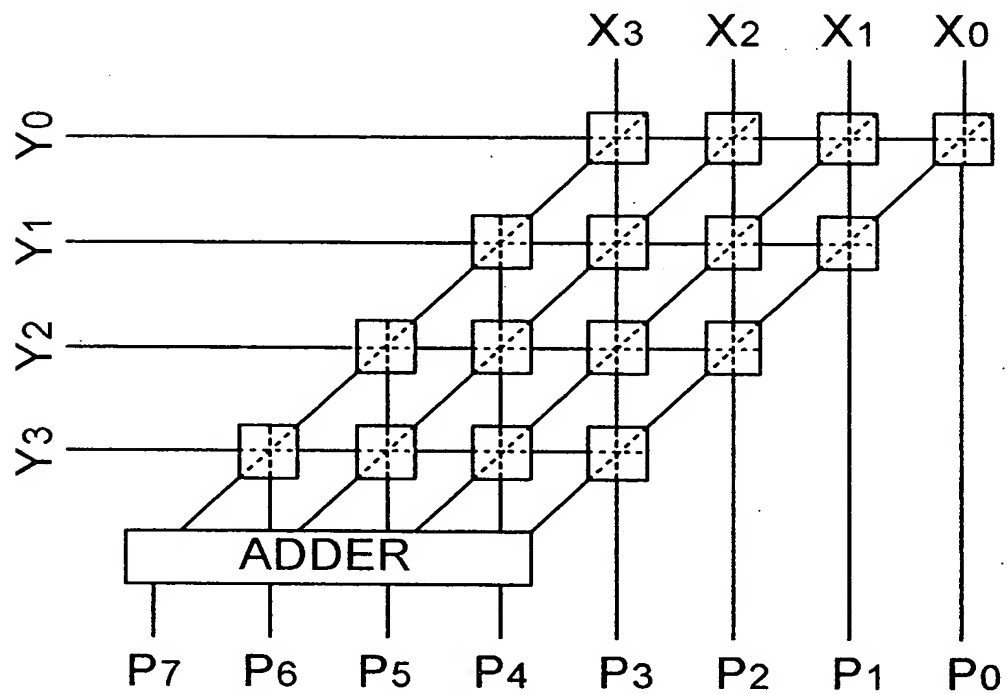
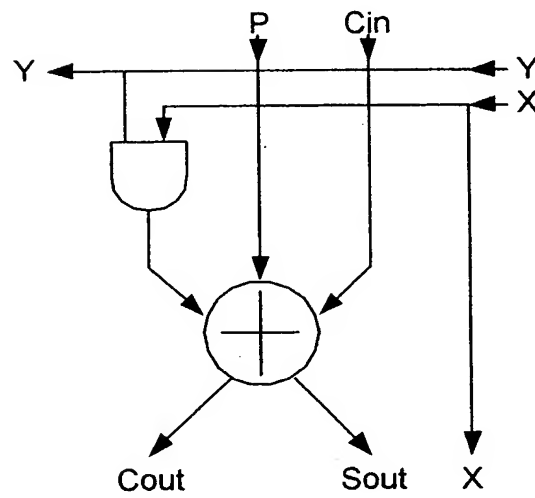
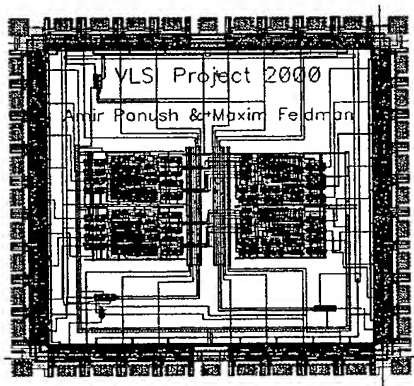


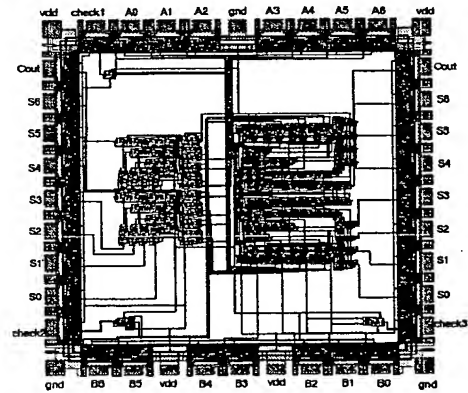
Fig. 23 – Prior art



**Fig. 24 – Prior art**



**a) GDI and prior art CMOS**



**b) GDI and prior art TG**

**Fig. 25**

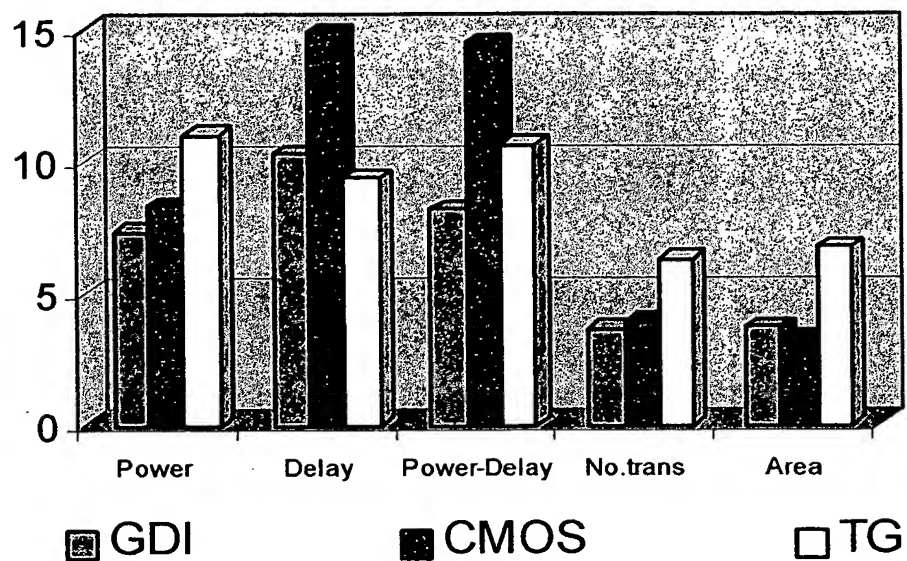


Fig. 26

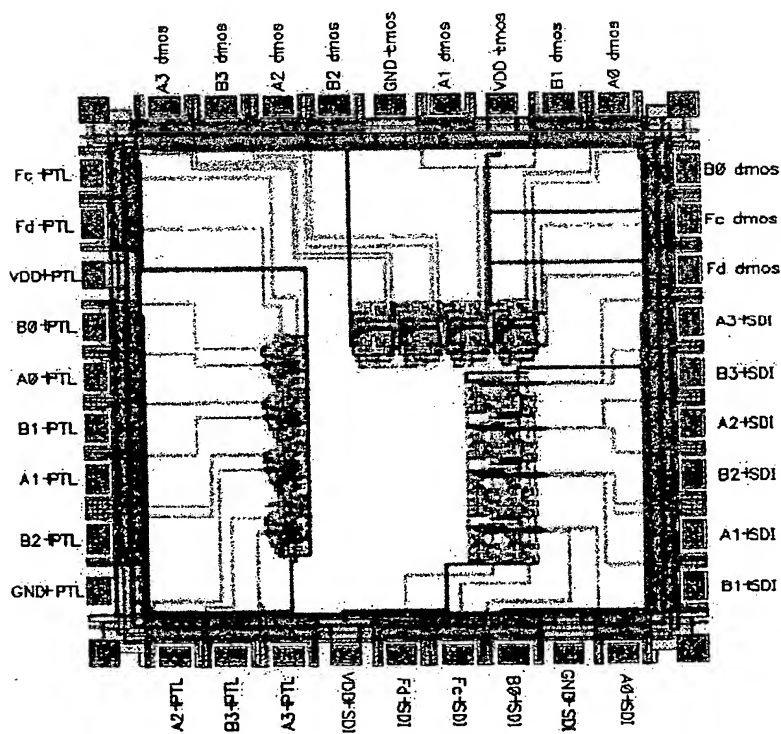


Fig. 27

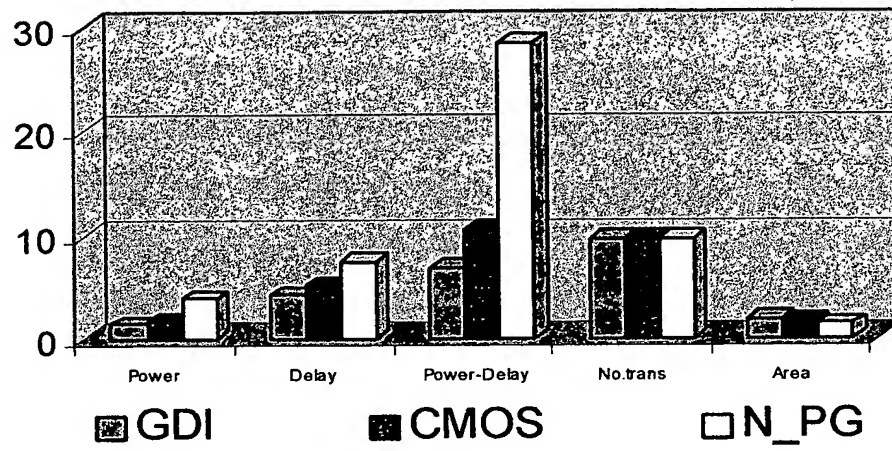


Fig. 28



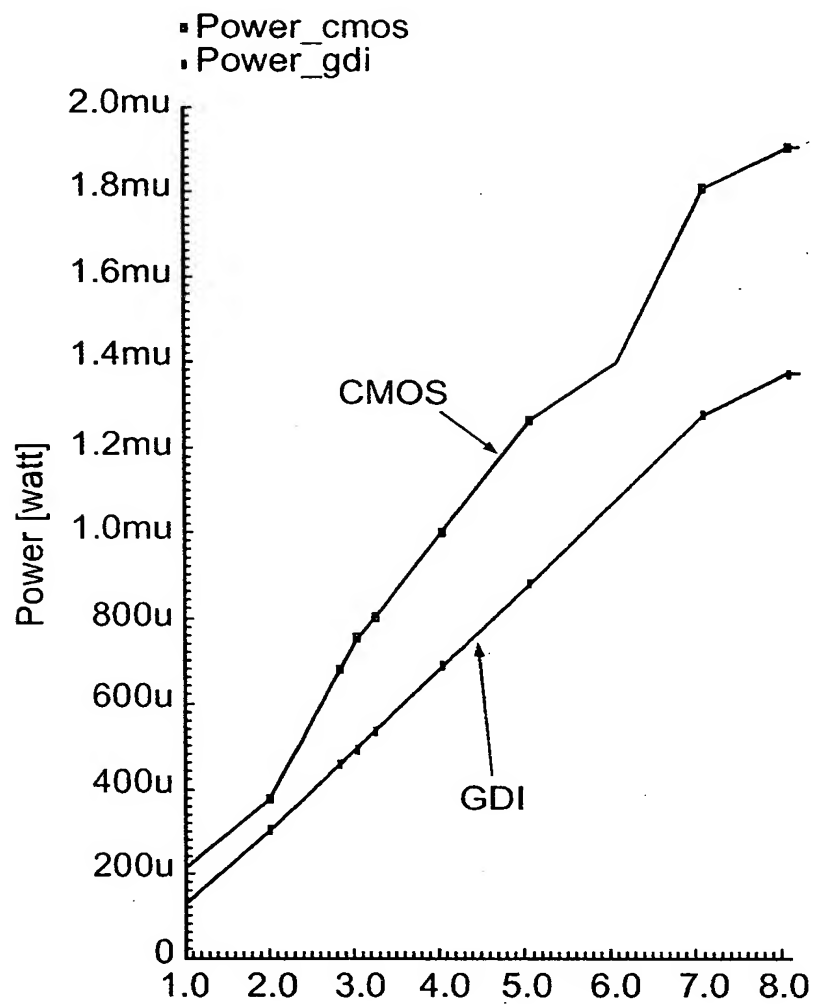


Fig. 29

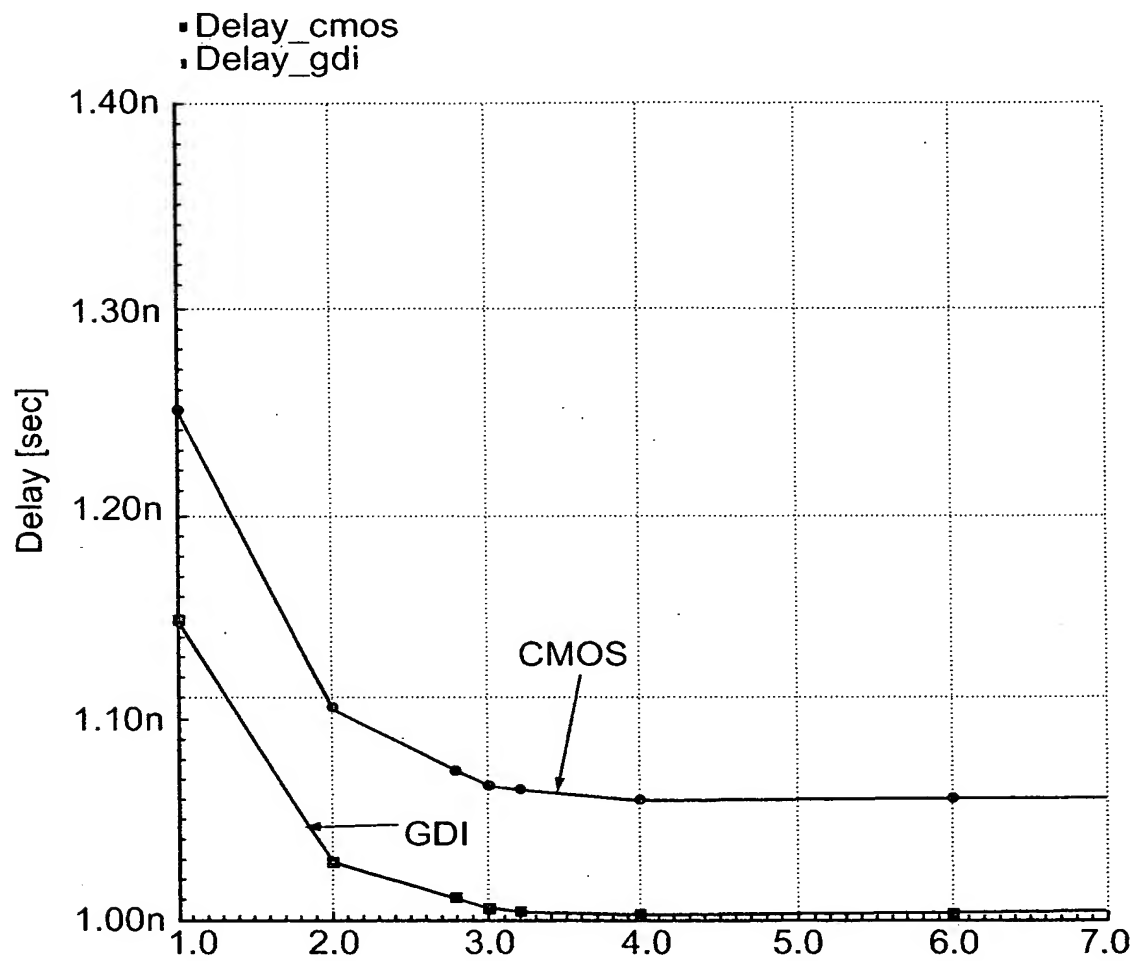


Fig. 30

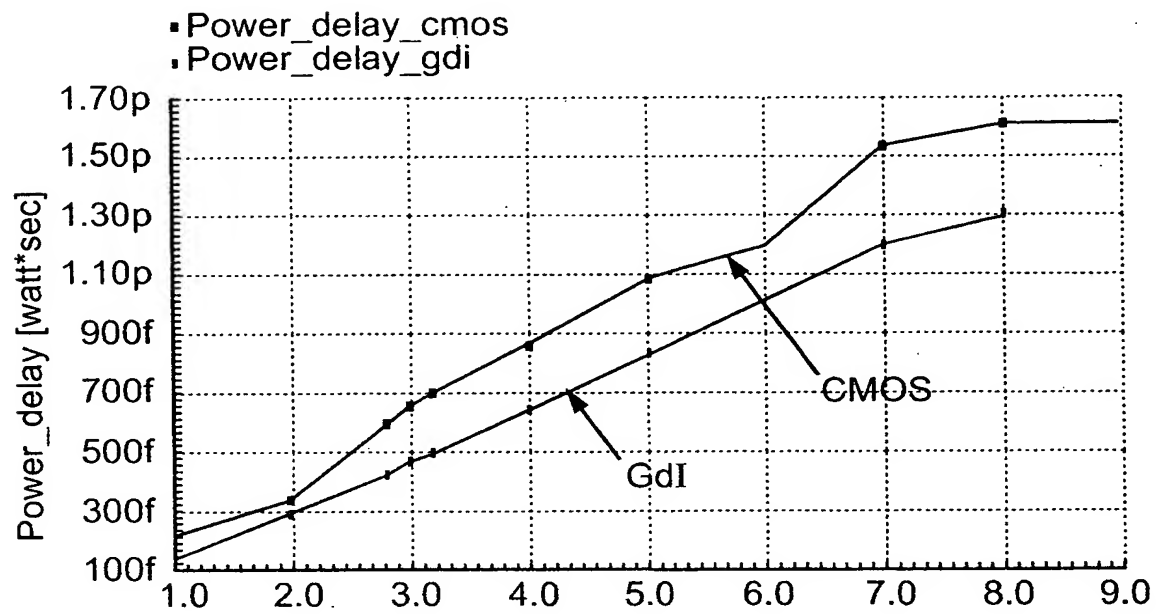
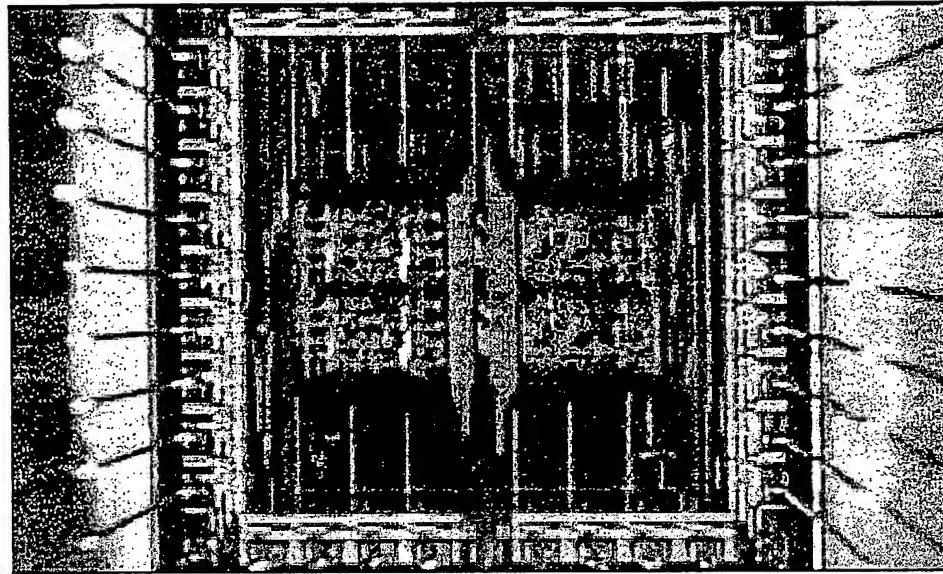


Fig. 31



**Fig. 32**

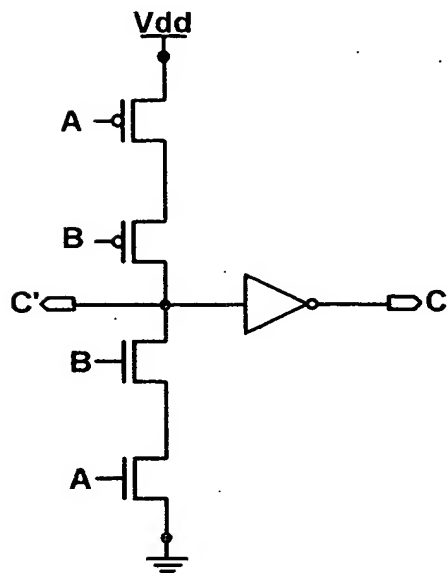


Fig. 33a - Prior art

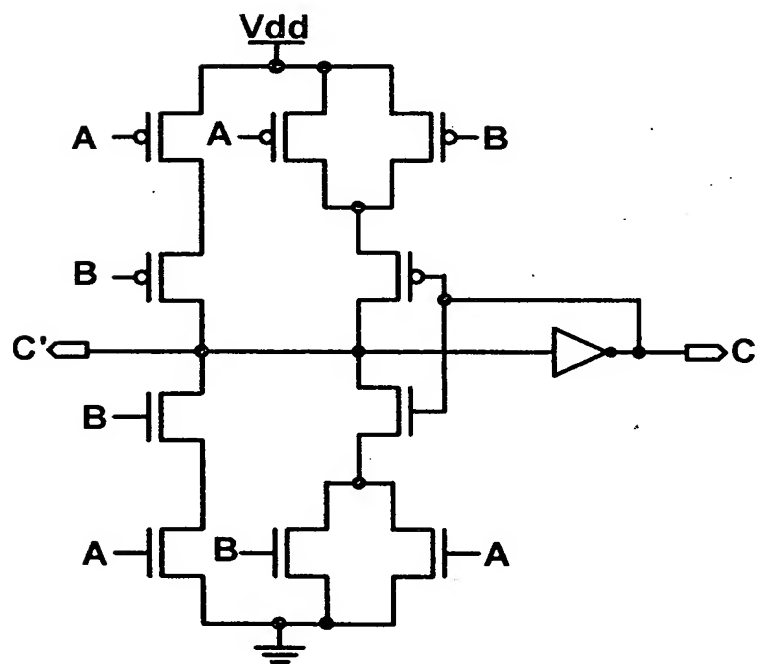


Fig. 33b - Prior art

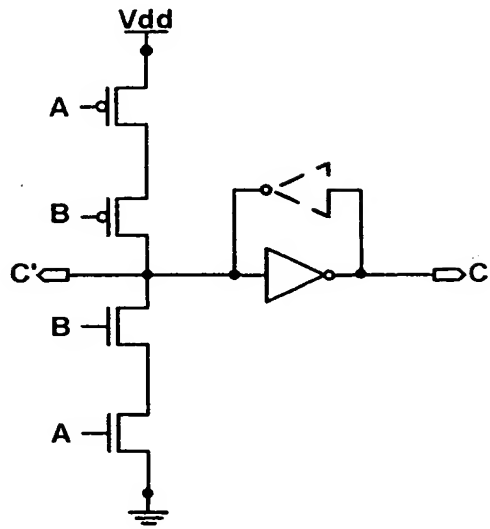


Fig. 33c - Prior art

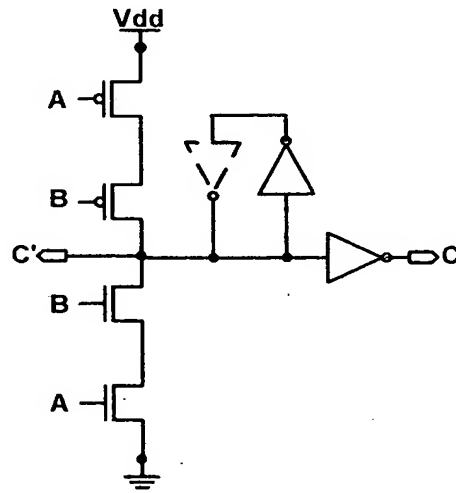


Fig. 33d - Prior art

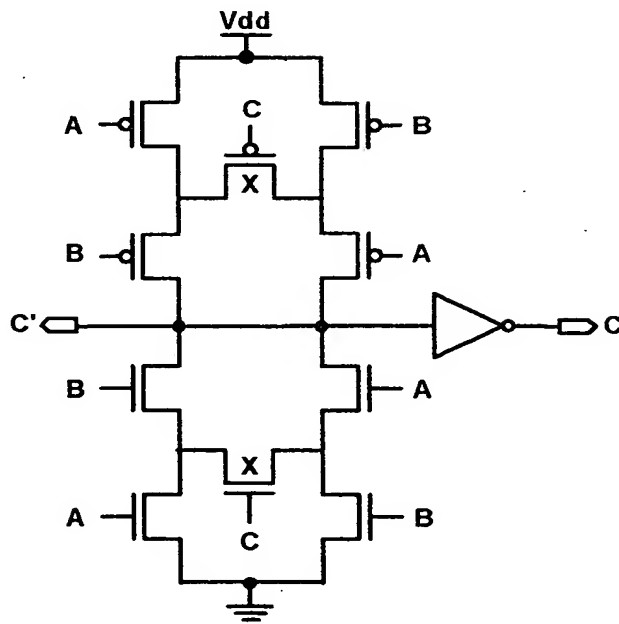
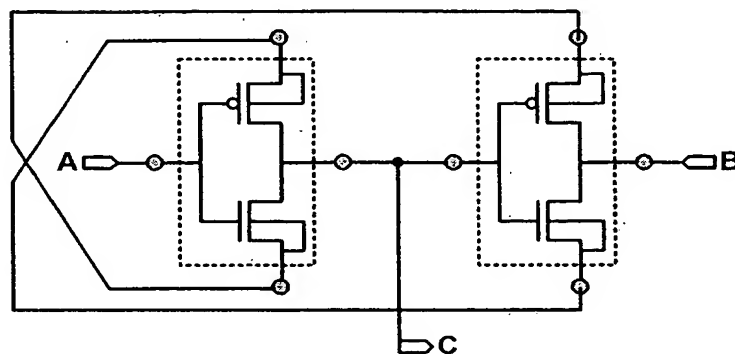
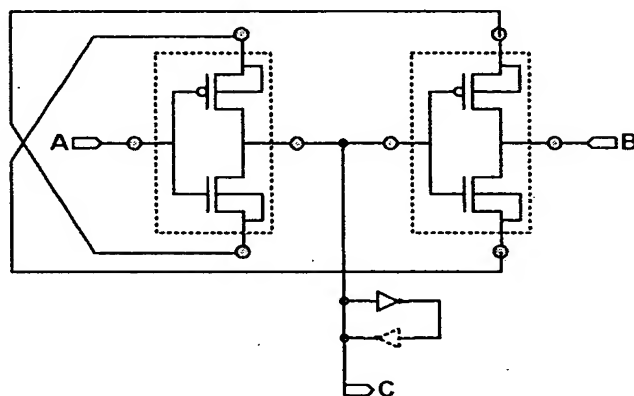


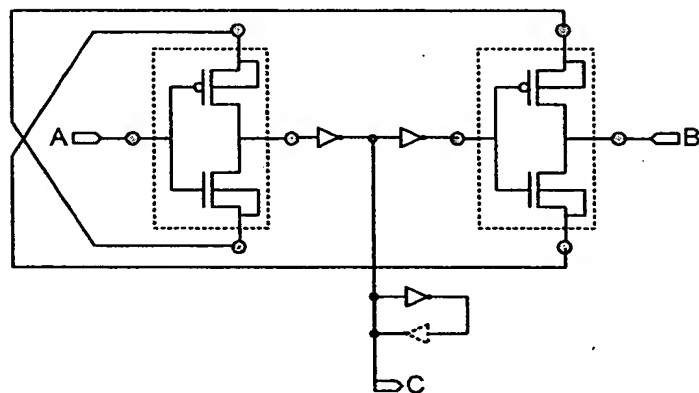
Fig. 33e - Prior art



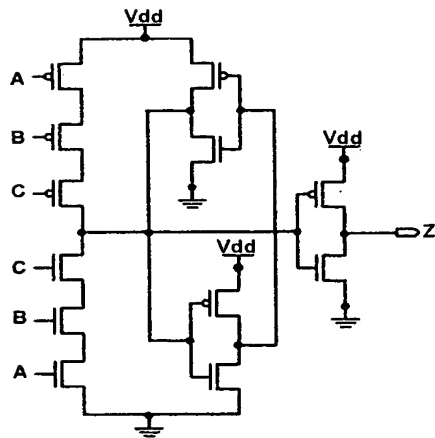
**Fig. 34a**



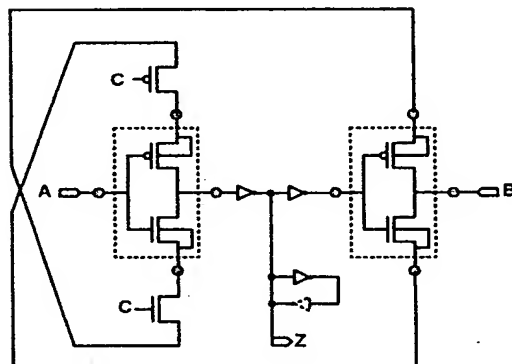
**Fig. 34b**



**Fig. 34c**

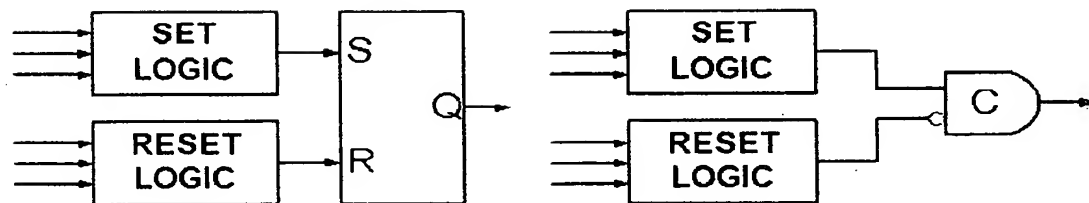


**Fig. 35a CMOS – Prior art**



**Fig. 35b GDI**



**Fig. 36 – Prior art**

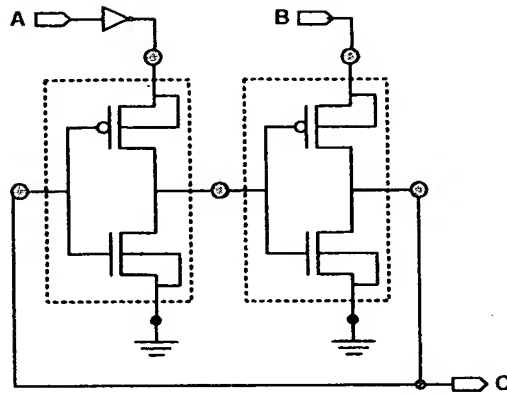


Fig. 37a

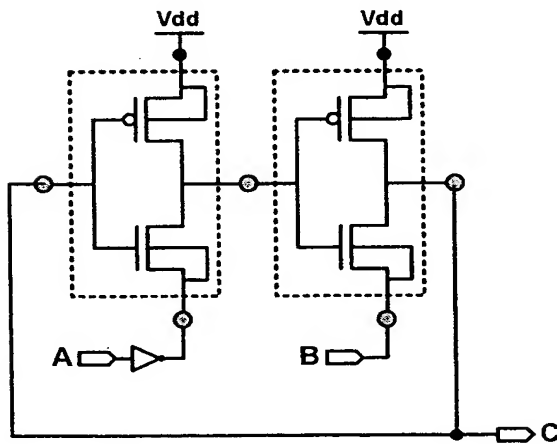
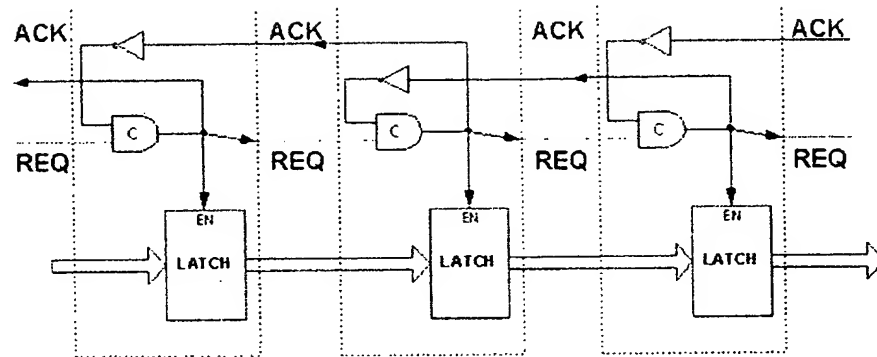
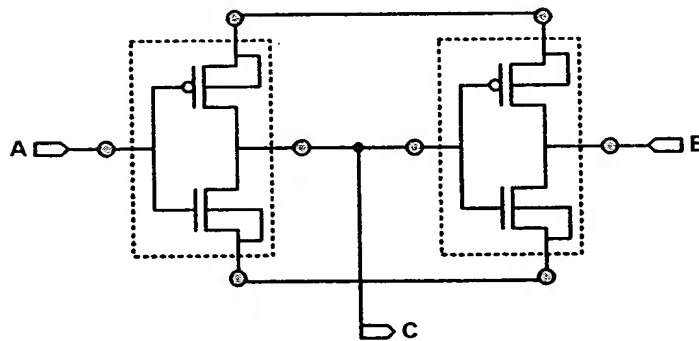


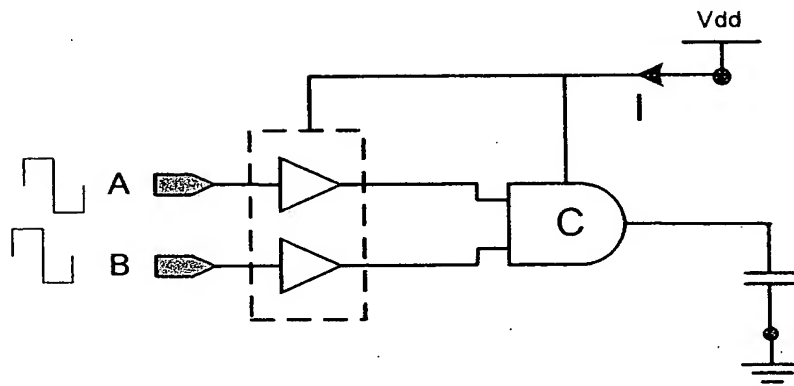
Fig. 37b



**Fig. 38 – Prior art**



**Fig. 39**



**Fig. 40**

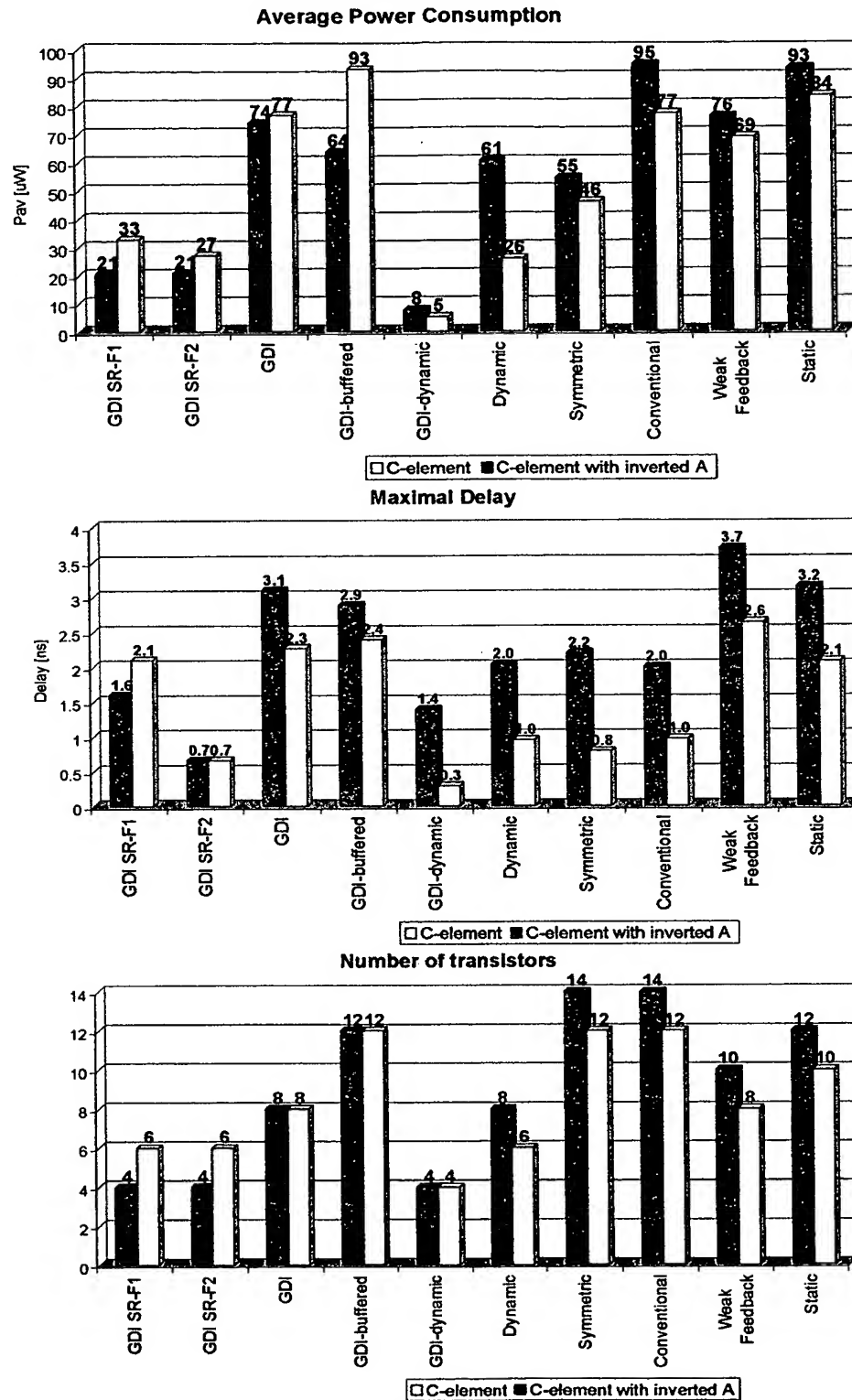


Fig. 41

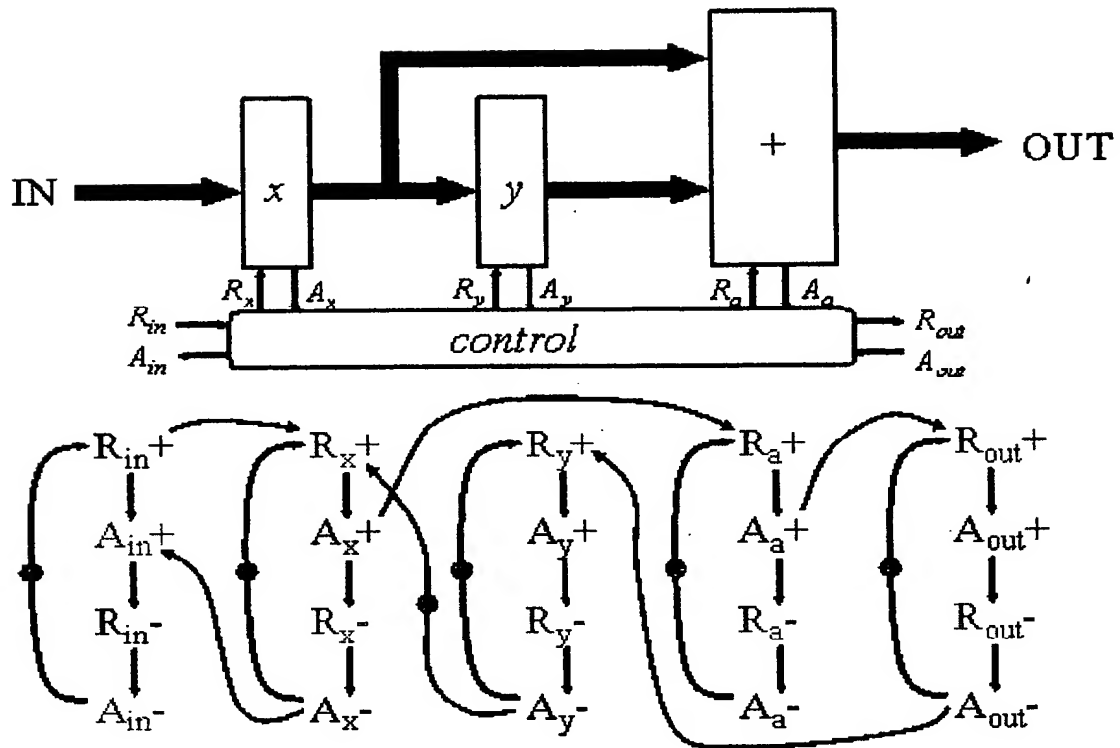
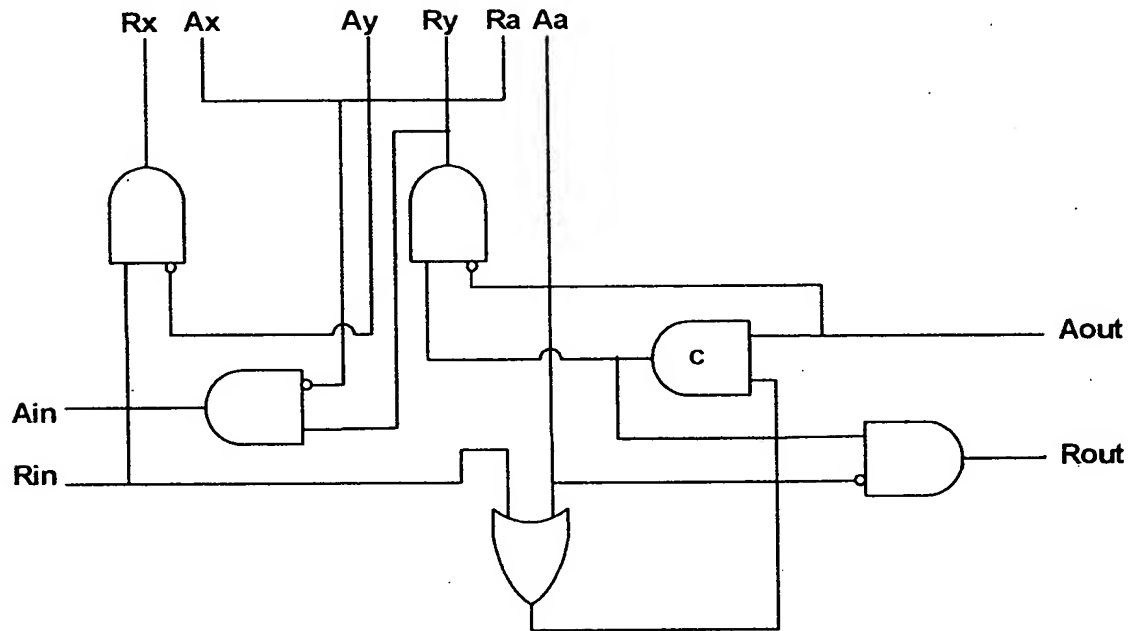
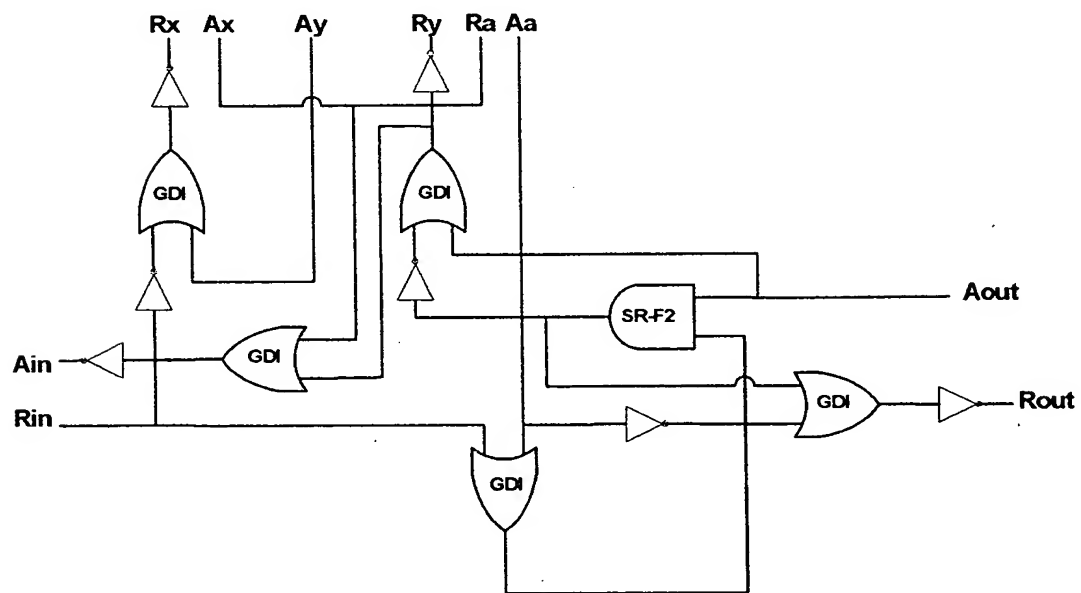
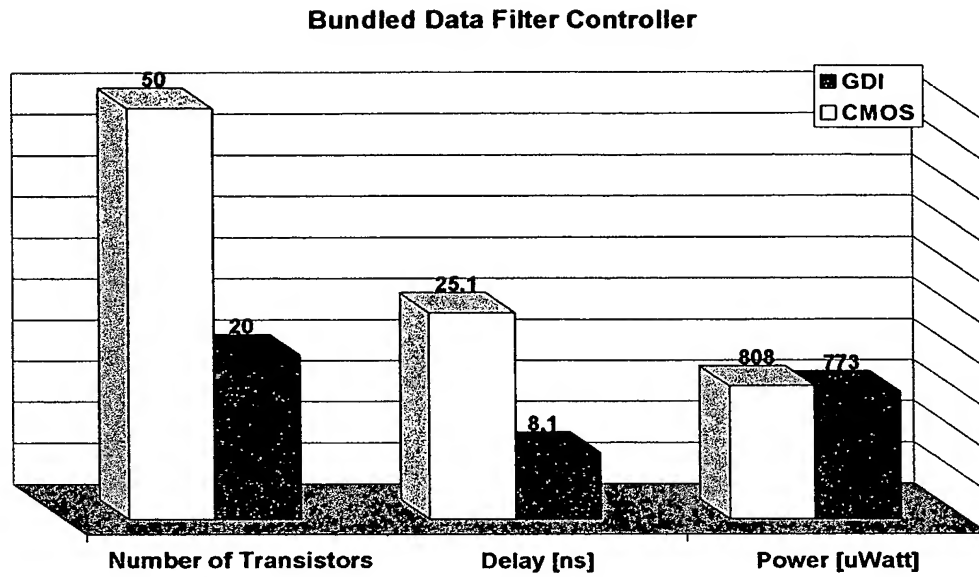
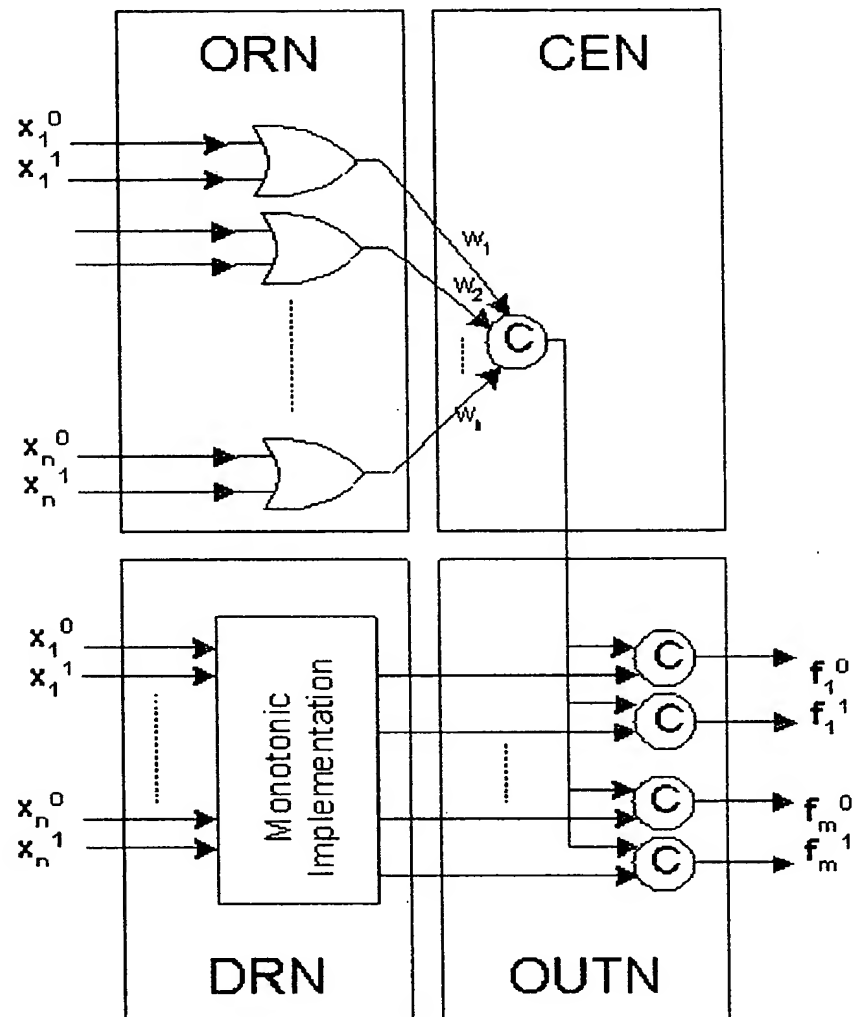


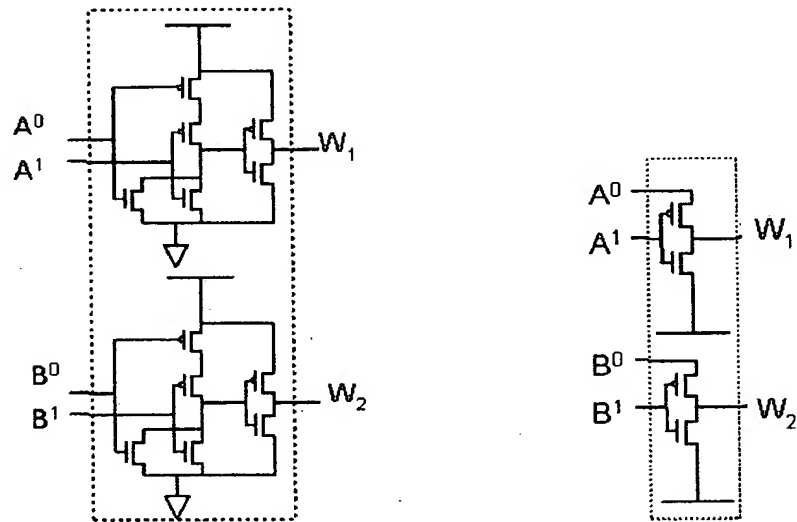
Fig. 42 – Prior art

**Fig. 43a – Prior art****Fig. 43b – Prior art**

**Fig. 44**



**Fig. 45 – Prior art**

**CMOS - Prior art****GDI****Fig. 46**

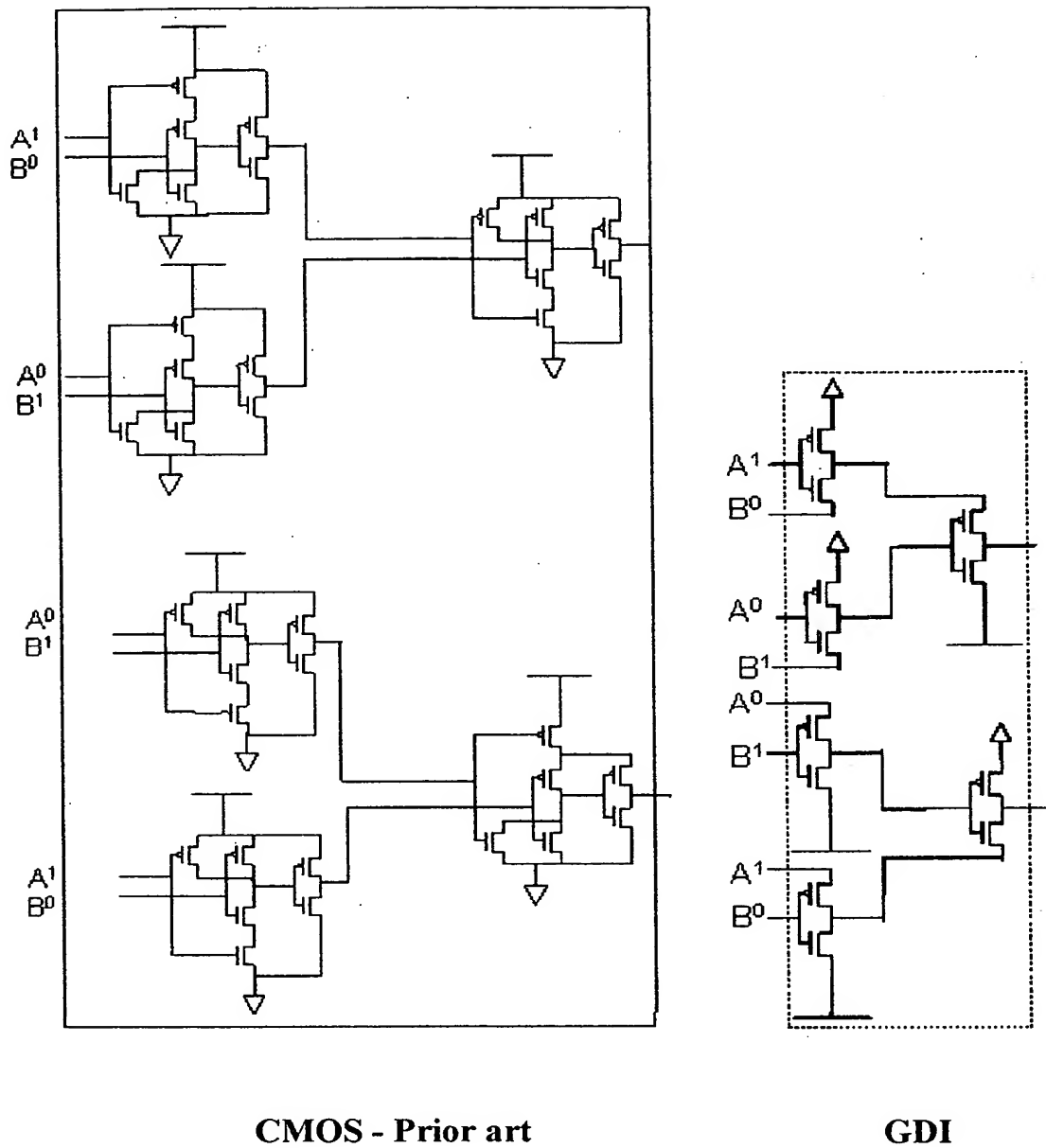


Fig. 47

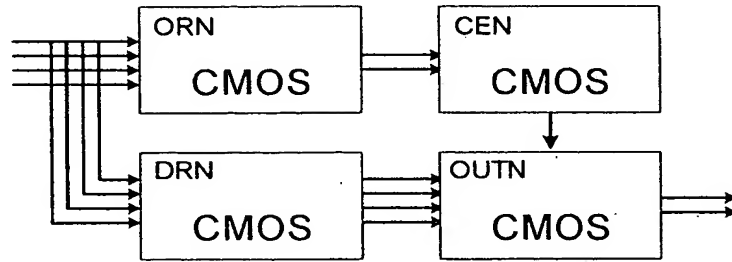


Fig. 48a

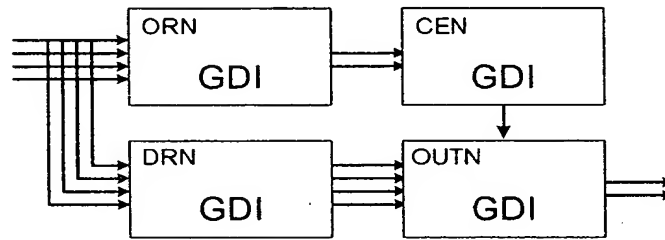


Fig. 48b

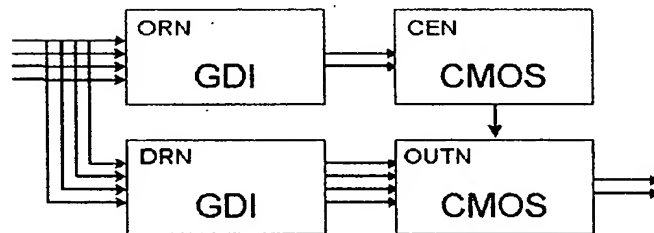
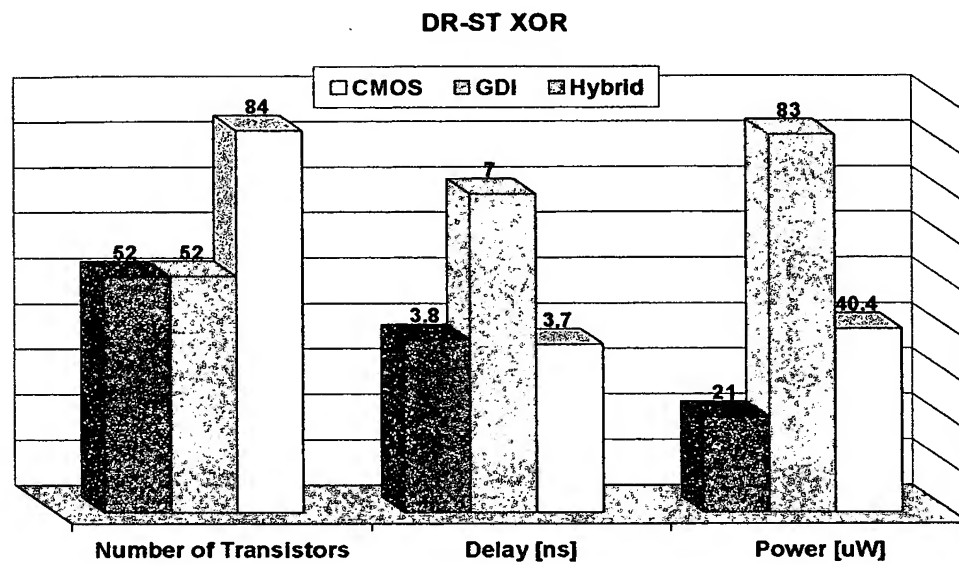


Fig. 48c

**Fig. 49**

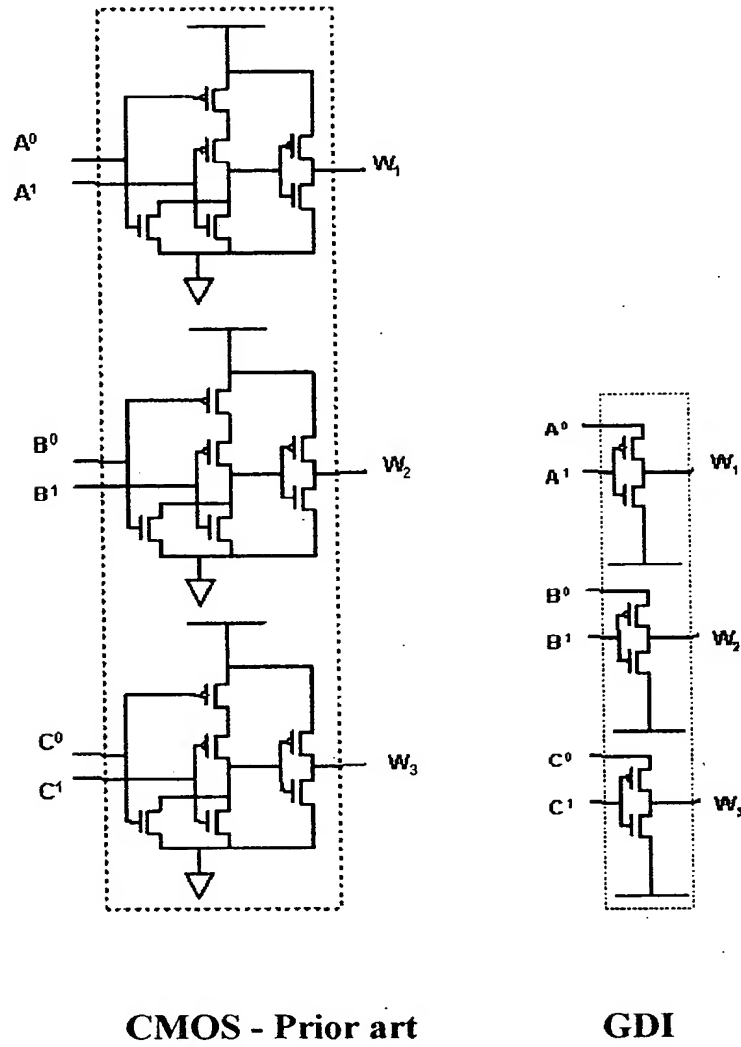


Fig. 50

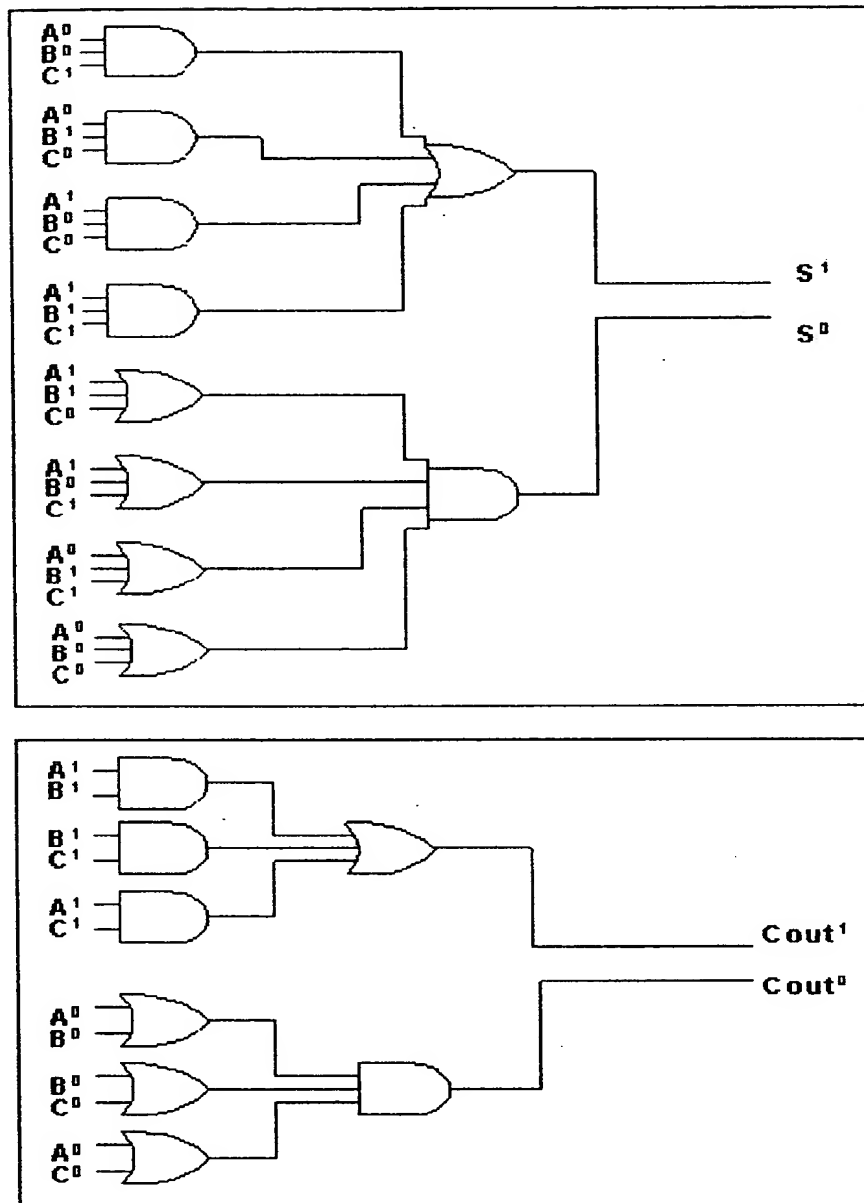
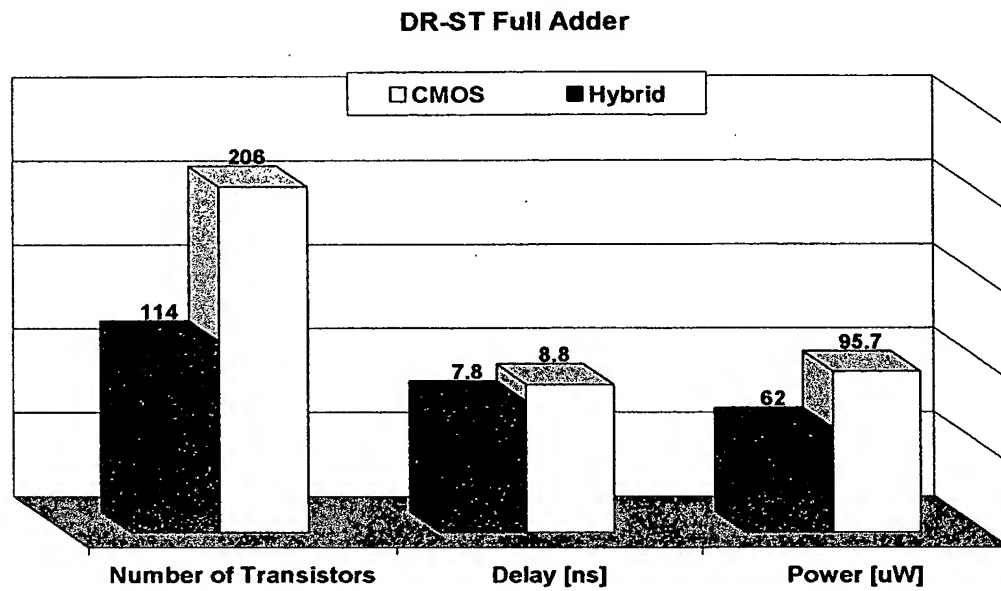
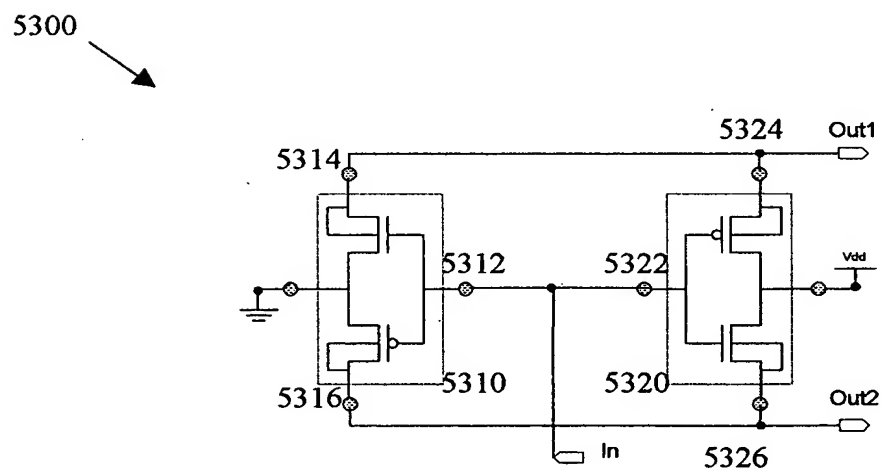


Fig. 51 – Prior art



**Fig. 52**



**Fig. 53**